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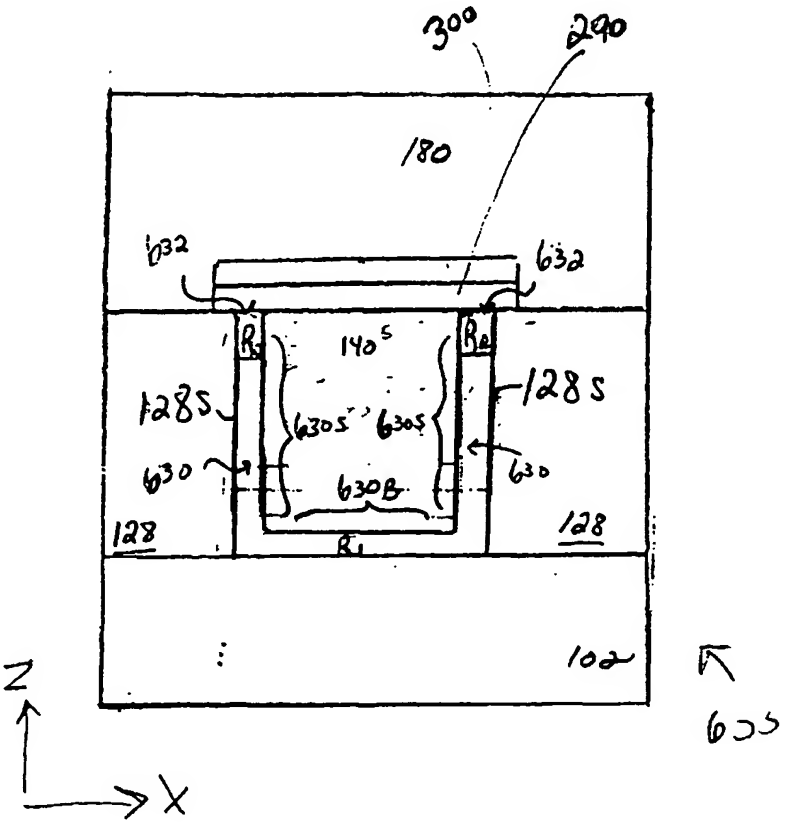

(57) Abstract: An electrically operated programmable resistance memory element. In one embodiment of the invention the memory element includes an electrical contact having at least a first region (R1) with a first resistivity and a second region (R2) with a second resitivity higher than the first resistivity. The more resistivity second region (R2) is preferably adjacent to the memory material (290). In another embodiment of the invention the memory element includes an electrical contact having a raised portion extending to an end adjacent to the memory material.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

ELECTRICALLY PROGRAMMABLE MEMORY ELEMENT

RELATED APPLICATION INFORMATION

This application is a continuation-in-part of U.S. Patent Application Serial Number 09/276,273, filed on March 25, 1999 which is a continuation-in-part of U.S. Patent Application Serial Number 08/942,000, filed October 1, 1997, now abandoned.

FIELD OF THE INVENTION

The present invention relates generally to a uniquely designed solid state, electrically operated memory element. More specifically, the present invention relates to programmable resistance memory elements.

BACKGROUND AND PRIOR ART

Programmable resistance memory elements formed from materials that can be programmed to exhibit at least a high or low stable ohmic state are known in the art. Such programmable resistance elements may be programmed to a high resistance state to store, for example, a logic ONE data bit. As well, they may be programmed to a low resistance state to store, for example, a logic ZERO data bit.

One type of material that can be used as the memory material for programmable resistance elements is phase change material. Phase change materials may be programmed between a first structural state where the material is generally more amorphous (less ordered) and a second

structural state where the material is generally more crystalline (more ordered). The term "amorphous", as used herein, refers to a condition which is relatively structurally less ordered or more disordered than a single crystal and has a detectable characteristic, such as high electrical resistivity. The term "crystalline", as used herein, refers to a condition which is relatively structurally more ordered than amorphous and has lower electrical resistivity than the amorphous state.

The concept of utilizing electrically programmable phase change materials for electronic memory applications is disclosed, for example, in U.S. Patent Nos. 3,271,591 and 3,530,441, the contents of which are incorporated herein by reference. The early phase change materials described in the '591 and '441 Patents were based on changes in local structural order. The changes in structural order were typically accompanied by atomic migration of certain species within the material. Such atomic migration between the amorphous and crystalline states made programming energies relatively high.

The electrical energy required to produce a detectable change in resistance in these materials was typically in the range of about a microjoule. This amount of energy must be delivered to each of the memory elements in the solid state matrix of rows and columns of memory cells. Such high energy requirements translate into high current carrying requirements for the address lines and for the

cell isolation/address device associated with each discrete memory element.

The high energy requirements for programming the memory cells described in the '591 and '441 patents limited the use of these cells as a direct and universal replacement for present computer memory applications, such as tape, floppy disks, magnetic or optical hard disk drives, solid state disk flash, DRAM, SRAM, and socket flash memory. In particular, low programming energy is important when the EEPROMs are used for large-scale archival storage. Used in this manner, the EEPROMs would replace the mechanical hard drives (such as magnetic or optical hard drives) of present computer systems. One of the main reasons for this replacement of conventional mechanical hard drives with EEPROM "hard drives" would be to reduce the power consumption of the mechanical systems. In the case of lap-top computers, this is of particular interest because the mechanical hard disk drive is one of the largest power consumers therein. Therefore, it would be advantageous to reduce this power load, thereby substantially increasing the operating time of the computer per charge of the power cells. However, if the EEPROM replacement for hard drives has high programming energy requirements (and high power requirements), the power savings may be inconsequential or at best unsubstantial. Therefore, any EEPROM which is to be considered a universal memory requires low programming energy.

The programming energy requirements of a programmable resistance memory element may be reduced in different ways. For example, the programming energies may be reduced by the appropriate selection of the composition of the memory material. An example of a phase change material having reduced energy requirements is described in U.S. Patent No. 5,166,758, the disclosure of which is incorporated by reference herein. Other examples of memory materials are provided in U.S. Patent Nos. 5,296,716, 5,414,271, 5,359,205, and 5,534,712 disclosures of which are all incorporated by reference herein.

The programming energy requirement may also be reduced through the appropriate modification of the electrical contacts used to deliver the programming energy to the memory material. For example, reduction in programming energy may be achieved by modifying the composition and/or shape and/or configuration (positioning relative to the memory material) of the electrical contacts. Examples of such "contact modification" are provided in U.S. Patent No. 5341,328, 5,406,509, 5,534,711, 5,536,947, 5,687,112, 5,933,365 all of which are incorporated by reference herein. Other examples are provided in U.S. Patent Application Serial No. 09/276,273 also incorporated by reference herein. Still further examples are provided in U.S. Patent Application Serial No. 09/620,318 also incorporated by reference herein.

SUMMARY OF THE INVENTION

One aspect of the present invention is an electrically operated memory element, comprising: a volume of memory material programmable to at least a first resistance state and a second resistance state; and an electrical contact in electrical communication with the memory material, the conductive sidewall spacer including at least a first region having a first resistivity and a second region having a second resistivity greater than the first resistivity.

Another aspect of the present invention is an method of forming a electrically operated memory element, comprising the steps of: providing a conductive material; increasing the resistivity of a portion of the conductive material; and depositing a memory material adjacent the portion.

Another aspect of the present invention is an electrically operated memory element, comprising: a programmable resistance memory material; and a conductive layer in electrical communication with the memory material, the conductive layer having a raised portion extending from an edge of the layer to a distal end adjacent the memory material.

Another aspect of the present invention is a method for making a programmable resistance memory element,

comprising: providing a conductive material; forming a sidewall spacer over a portion of the conductive material; removing a portion of the conductive material to form a raised portion extending from the conductive material under the spacer; and forming a programmable resistance material adjacent to at least a portion of the raised portion.

Another aspect of the present invention is a method for making a programmable resistance memory element, comprising: providing a conductive layer; forming a raised portion extending from an edge of the conductive layer; and forming a programmable resistance material adjacent to at a least a portion of the raised portion.

Another aspect of the present invention is a method of forming a programmable resistance memory element, comprising: providing a first dielectric layer; forming a sidewall surface in the dielectric layer; forming a conductive layer on the sidewall surface; forming a second dielectric layer over the conductive layer; forming or exposing an edge of the conductive layer; forming a raised portion extending from the edge of the conductive layer; and forming a programmable resistance material adjacent to at least a portion of the raised portion.

Another aspect of the present invention is a method for making an electrode for a semiconductor device, comprising: providing a conductive layer; and forming a raised portion extending from an edge of the conductive layer.

Another aspect of the present invention is a method of making an electrode for a semiconductor device, comprising: providing a first dielectric layer; forming a sidewall surface in the dielectric layer; forming a conductive layer on the sidewall surface; forming a second dielectric layer over the conductive layer; forming or exposing an edge of the conductive layer; and forming a raised portion extending from the edge of the conductive layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a cross-sectional view of a memory device of the present invention comprising conductive sidewall spacers;

Figure 1B is a three-dimensional view of a portion of the memory device of Figure 1A;

Figure 1C is a cross-sectional view of a memory device of the present invention comprising conductive sidewall spacers on an angled sidewall;

Figure 1D is a cross-sectional of a memory device of the present invention comprising multi-regioned conductive sidewall spacers;

Figure 1E shows a memory device having an intermediate layer disposed between the memory material and the conductive sidewall spacers;

Figure 1F shows a memory device wherein the conductive sidewall spacers have an additional region R3 adjacent to the memory material;

Figures 2A-2H show a process for making a memory device having multi-region conductive spacers as electrical contacts;

Figure 2A'-2D' show an alternate process for making a memory device having multi-region conductive spacers as electrical contacts;

Figure 3A is a three-dimensional view of a memory device of the present invention having a conductive sidewall spacer as an electrical contact;

Figure 3B is a three-dimensional view of a memory device of the present invention having a multi-region cylindrically shaped conductive sidewall spacer as an electrical contact;

Figure 4A is a conductive liner formed in a trench;

Figure 4B is a conductive liner formed in a rectangular opening;

Figure 4C is a conductive liner formed in a circular opening;

Figure 5A is a three-dimensional view of a memory device having a conductive liner as an electrical contact;

Figure 5B is a cross-sectional view of the memory device from Figure 5A;

Figure 5C is a three-dimensional view of a memory device having a multi-region conductive liner as an electrical contact;

Figure 5D is a cross-sectional view of the memory device from Figure 5C;

Figures 6A-6G is a process for making a memory device of the present invention having a multi-region conductive liner as an electrical contact;

Figure 7A is a three-dimensional view of a memory element of the present invention having a horizontally disposed contact layer edgewise adjacent to a volume of memory material;

Figure 7B is a cross-sectional view of the memory element from Figure 7A;

Figure 8 is a cross-sectional view of a memory element having a multi-regioned electrical contact;

Figure 9A is a cross-sectional view of a memory device of the present invention comprising conductive sidewall spacers;

Figure 9B is a three-dimensional view of a portion of the memory device of Figure 9A;

Figure 9C is a cross-sectional view of a memory element having a raised portion extending to a distal end adjacent the memory material;

Figure 9D is a three-dimensional view of conductive sidewall spacers with rapier modification;

Figures 10A-10S shows a process for making the memory element of Figure 9C;

Figure 11 is a cross-sectional view (parallel to y-z plane) of a multi-regioned sidewall spacer with a raised portion;

Figure 12A is a three-dimensional view of a memory

device having a cylindrically shaped conductive sidewall spacer as an electrical contact;

Figure 12B is a three-dimensional view of cylindrically shaped conductive sidewall spacer with raised portions extending from the top edge of the sidewall spacer;

Figure 12C is a side view of a memory element using the electrical contact from Figure 3B;

Figure 13A is a memory element having a conductive liner as an electrical contact;

Figure 13B is a cross-sectional view of the memory element of Figure 13A;

Figure 13C is a three-dimensional view of a cylindrically shaped conductive liner with raised portions extending from the top edge of the conductive liner;

Figure 13D is a side view of a memory element incorporating the electrical contact from Figure 13C;

Figures 14A-14S' is an embodiment of a process for making a memory element shown in Figure 13D; and

Figure 15 is an example of a conductive liner with raised portions extending from a top edge of the liner's sidewall layers.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to programmable resistance memory elements. The memory element comprises a volume of memory material which is programmable between at

least a first resistance state and a second resistance state in response to an electrical signal. The memory element further comprises a means of delivering the electrical signal to the volume of memory material. Preferably, the means of delivering the electrical signal comprises a first and a second electrical contact in electrical communication with the volume of memory material.

In a first embodiment of the present invention, at least one of the electrical contacts is a conductive sidewall spacer. The conductive sidewall spacer is in electrical communication with the volume of memory material. As will be explained in more detail below, it is preferable that substantially all of said electrical communication is through at least a portion of an edge of the conductive sidewall spacer. That is, substantially all of the electrical communication is through an edge or a portion of an edge of the conductive sidewall spacer. It is noted that, as used herein, the terminologies "at least a portion of an edge", "an edge or a portion of an edge", "all or a portion of an edge", and "edge portion" all mean the same and may be used interchangeably.

Figure 1A is an example of this first embodiment. Shown is a cross-sectional view of a memory device 100 of the present invention formed on a semiconductor substrate 102. The cross-sectional view is parallel to the x-z plane. The x-dimension is referred to as the "channel

length" or simply the "length" of the memory device 100. The y-z plane of the memory device (not shown in Figure 1A) is perpendicular to the plane of the illustration. The y-dimension is referred to as the "channel width" or simply the "width" of the memory device.

In the example shown, the memory device 100 comprises two independent single-cell memory elements. The first memory element comprises a first contact 130A, a layer of memory material 290 and a second contact 300. The second memory element comprises a first contact 130B, a layer of memory material 290 and a second contact 300.

In the example shown, the volume of memory material is a substantially horizontally disposed layer of memory material 290. As shown, the layer of memory material 290 and the second contact 300 are shared by the first and second memory elements. However, other embodiments are possible where each memory element has a unique corresponding volume (or layer) of memory material and a unique corresponding second contact. The dielectric region 140 electrically isolates the electrical contact 130A from the electrical contact 130B. An upper dielectric region 180 is deposited on top of the memory device 100. The upper dielectric layer 180 may comprise boron-phosphate silica glass (BPSG).

Each of the electrical contacts 130A and 130B is in the form of a conductive sidewall spacer. As used herein, reference to the "conductive sidewall spacer

130A,B" (in the singular) refers to either conductive spacer 130A or conductive spacer 130B. Reference to the "conductive sidewall spacers 130A,B" (in the plural) refers to both conductive spacers 130A and 130B of device 100.

In the example shown, each conductive sidewall spacer 130A,B is "single-layered". That is, each conductive spacer 130A,B is a single, substantially vertically disposed, sidewall layer. Each sidewall layer may be formed by the substantial conformal deposition of a conductive material onto a sidewall surface 128S. (In Figure 1A, sidewall surfaces 128S and bottom surface 106 form a trench extending perpendicular to the plane of the illustration of Figure 1A). A "single-layered" conductive spacer is distinguishable from a "multi-layered" conductive spacer where one or more additional sidewall layers are substantially conformally deposited onto the surface of an existing sidewall layer.

In the example shown in Figure 1A, the layer of memory material 290 is deposited onto the conductive spacer 130A,B so that only the top end 132 of the conductive spacer 130A,B is adjacent to the memory material 290. The remainder of the conductive spacer is remote to the memory material. Hence, substantially all electrical communication between the conductive spacer 130A,B and the memory material 290 is through the top end 132 of the conductive spacer. As used herein, the terminology

"above" and "below" as well as the terminology "top" and "bottom" are defined in terms of relative distances from the substrate. The terminology is independent of the orientation of the substrate.

In the embodiment in Figure 1A, the top end of the conductive spacer 130A,B is an edge of the conductive spacer (i.e., the "top edge"). An example of an edge of a layer is a surface substantially parallel to the thickness dimension of the layer (where the thickness is preferably the layer's smallest dimension). In the embodiment shown in Figure 1A, the conductive sidewall spacer 130A,B is a substantially vertically disposed sidewall layer. Hence, the thickness "t" of the conductive spacer 130A,B, as shown in Figure 1A, is the dimension of the sidewall layer substantially parallel to the x-dimension or channel length. In the example shown in Figure 1A, the top edge 132 is a surface substantially parallel to the substrate 102. The thickness "t" may have a dimension which is less than that which can be achieved by conventional photolithographic techniques.

Figure 1B is a highly idealized three-dimensional view of the conductive spacer 130A,B showing its thickness "t", width "w" and a height "h". As noted above, the thickness "t" of the conductive sidewall spacer 130A,B is the dimension of the spacer along the x-dimension or channel length (parallel to plane of the illustration). The width "w" is the dimension of the conductive spacer along the y-

dimension or channel width (perpendicular to the plane of the illustration of Figure 1A). The height "h" is the distance above the substrate 102.

The top edge 132 of each conductive spacer 130A,B is adjacent to the memory material 290 while the remainder of each conductive spacer is remote to the memory material. Hence, substantially all electrical communication between the conductive spacer 130A,B and the memory material 290 is through at least a portion of the top edge 132. That is, substantially all electrical communication is through all or a portion of the top edge 132. It is noted that the top edge 132 need not be in actually contact with the memory material.

In the embodiment shown in Figure 1A, the memory material 290 is adjacent to the entire top edge 132 of both conductive spacers 130A,B. However, in an alternate configuration it is possible to position the layer 290 of memory material so that it is adjacent to the top edge 132 of only one of the conductive spacers. In yet another configuration, it is possible to position the layer 290 of memory material so that only a portion of the top edge 132 of one or both of the conductive spacers 130A,B is adjacent to the memory material.

In the embodiment shown in Figure 1A, the conductive spacers 130A,B are sidewall layers which are substantially vertically disposed and thus substantially perpendicular to the layer of memory material 290 and to the substrate. It

is, of course, also possible that the conductive spacers 130A,B be "tilted" so that they are not substantially perpendicular to the memory material. As shown in Figure 1C, the sidewall layers 130A,B may be formed on "angled" sidewall surfaces 128s (for example, the sidewall spacers 130A,B could be formed in a V-shaped trench). This type of structure is also within the spirit and scope of the present invention. The surfaces 132 shown in Figure 1C (substantially parallel to the substrate) are also considered "edges" of the conductive sidewall spacers 130A,B of Figure 1C.

As seen, the layers 130A,B form an angle of incidence "THETA" with the layer of memory material 290. Preferably, THETA is greater than 30° and less than 150°. More preferably, THETA is greater than 45° and less than 135°. Most preferably, THETA is greater than 60° and less than 120°.

It is further noted that yet other configurations are possible where the memory material is positioned adjacent to the bottom edge or a portion of the bottom edge of the conductive spacer. In yet another configuration, it is possible that the memory material is adjacent only to a side edge or a portion of a side edge of one or both of the conductive spacers. Referring again to Figure 1B, the "side edges" of each conductive spacer 130A,B are the surfaces defined by the thickness "t" and the height "h".

Hence, it is preferable that the conductive spacer is

"edgewise adjacent" to the memory material. That is, only an edge or a portion of an edge of the conductive spacer 130A,B is adjacent to the memory material. Substantially all of the remainder of the conductive spacer is remote to the memory material. Preferably, substantially all of the electrical communication between the conductive sidewall spacer is through an edge of the conductive spacer or a portion of an edge. That is, it is preferable that substantially all electrical communication is through at least a portion of an edge (i.e., an "edge portion") of the conductive sidewall spacer.

As used herein the terminology "area of contact" is the portion of the surface of an electrical contact through which the electrical contact electrically communicates with the memory material. As noted, it is preferable that substantially all electrical communication between the memory material 290 and a conductive sidewall spacer 130A,B occurs through all or a portion of an edge of the conductive spacer (for example, through all or a portion of the top edge 132). Hence, the area of contact between the conductive spacer 130A,B and the memory material 290 is an edge of the conductive sidewall spacer or a portion of an edge of the conductive sidewall spacer. That is, the area of contact between the conductive spacer and the memory material is an "edge portion" of the conductive sidewall spacer. It is again noted that the conductive spacer need not actually physically contact the memory material. It is

sufficient that the conductive spacer is in electrical communication with the memory material. The area of contact, being only an edge portion (i.e., an edge or a portion of an edge) of the conductive spacer, is thus very small and is proportional to the thickness of the conductive spacer.

Referring now to Figure 1D, it is seen that in one embodiment of the invention it is possible that each conductive sidewall spacer 130A,B is "multi-regioned". That is, each single sidewall layer 130A,B comprises at least a first region R1 having a first resistivity and a second region R2 having a second resistivity. The resistivity of the second region R2 is greater than the resistivity of the first region R1.

In general, the first and second regions may be positioned anywhere within the conductive sidewall spacer. There are many different ways of positioning the regions within the conductive sidewall spacer (that is, many different configurations are possible). In one possible configuration, it is preferable that more resistive second region R2 is adjacent to the memory material while the less resistant first region R1 is remote to the memory material.

In a second possible configuration, the more resistive second region R2 may be adjacent to the area of contact between the memory material and the conductive

spacer while the less resistive first region R1 may be remote to the area of contact. In a third possible configuration, the more resistive second region may be adjacent to an edge of the conductive spacer while the (for example, the top edge) and the less resistive first region may be remote to this edge.

As noted above, the area of contact between the memory material and the conductive spacer may be an edge portion of the conductive spacer. Hence, the more resistive region R2 may be positioned adjacent to the edge portion defining the area of contact and the less resistive region R1 may be positioned remote to the edge portion defining the area of contact.

Certain embodiments of the memory element may satisfy more than one of the configurations discussed above. Other configurations are also possible. Furthermore, while the possible ways of positioning the first and second regions R1, R2 was discussed in regards to a conductive sidewall spacer, the discussion is applicable to all embodiments of the present invention. For example, the discussion is applicable to the conductive liners and contact layers discussed below.

The more resistive second region R2 is a portion of the conductive sidewall layer. Preferably, this portion of the sidewall layer (that is, this "layer portion") includes at least a portion of an edge of the sidewall

layer (that is, the more resistive sidewall layer portion R2 preferably includes an "edge portion" of the sidewall layer). In the example shown in Figure 1A, the more resistive second region R2 is a "top portion" of the conductive spacer that includes the top edge 132 (and remote to substrate 102). That is, it extends from the top edge 132 downwardly (i.e., toward the substrate 102) into the interior of the conductive spacer for some distance "h2" (the "height" of the more resistive section region R2). The distance "h2" is not fixed. It may be very small, for example, between about 10 to about 20 Angstroms. In this case, the more resistive top portion is essentially the surface defined by all or a portion of the top edge. Alternately, the distance "h2" may extend further below the top edge 132 and into the interior of the conductive spacer. For example, the distance "h2" may be about 500 Angstroms to about 600 Angstroms. The height "h2" of the regions R2 are preferably less than about 1000 Angstroms, more preferably less than about 800 Angstroms, and most preferably less than about 600 Angstroms.

The less resistive region R1 is remote to the top edge 132. In the example shown, it extends from the bottom of the first region R2 to the substrate 102. The height "h1" of the first region R1 is indicated in Figure 1A. The height of regions R1 is preferably less than about 10,000 Angstroms, more preferably, less than about 7,000 Angstroms, most preferably less than about 5,000 Angstroms.

In is noted that in the configuration shown in Figure 1A, the region R1, region R2 and the memory material are is electrical series. It is further noted that in the embodiment shown in Figure 1A, conductive sidewall spacer 130A,B comprises only two regions R1 and R2. However, in other embodiments, one or both of the conductive spacers 130A,B may comprise more than two regions of material.

Examples of materials which may be used for the more resistive second region R2 include n-type doped polysilicon,
p-type doped polysilicon, n-type doped silicon carbon compounds and/or alloys, p-type doped silicon carbon compounds and/or alloys, titanium carbon-nitride, titanium aluminum nitride, titanium silicon-nitride, carbon, and forms of titanium nitride.

Examples of materials which may be used for the less resistive first region R1 include n-type doped polysilicon, p-type doped polysilicon, n-type doped silicon carbide, p-type doped silicon carbide, titanium-tungsten, tungsten silicide, tungsten, molydenum, and titanium nitride.

In the memory device 100 shown in Figure 1A, each of the conductive sidewall spacers 130A,B delivers electrical current to the memory material. As the electrical current passes through the conductive sidewall spacers and through the memory material, at least a portion of the electric potential energy of the electrons is transferred to the

surrounding material as heat. That is, the electrical energy is converted to heat energy via Joule heating. The amount of electrical energy converted to heat energy (that is, the amount of Joule heating) increases with the resistivity of the material as well as with the current density passing through the material.

As discussed above, the conductive sidewall spacers of the present invention may be formed having a more resistive material adjacent to the memory material and a less resistive material remote to the memory material. Hence, there is relatively high power dissipation from Joule heating in region R2 of each conductive spacer adjacent to the memory material. Also, there is relatively low power dissipation from Joule heating in region R1 of each conductive spacer remote to the memory material. The multi-region sidewall spacer may be referred to as a "matchstick" contact. It has a relatively "cooler" bottom portion R1 and relatively "hotter" top portion R2. While not wishing to be bound by theory, it is believed that dissipating power in the electrical contact from Joule heating adjacent to the memory material may at least partially assist (or may even dominate) the programming of the memory material. It is also believed that dissipating power in the electrical contact remote to the memory material may actually waste power and increase the total energy needed to program the memory material. Hence, providing an electrical contact structure having a

relatively high power dissipation adjacent to the memory material and a relatively low power dissipation remote to the memory material may thus decrease the total power and energy needed to program the memory device.

Furthermore, as noted above, the conductive sidewall spacer may be edgewise adjacent to the memory material and the area of contact between the memory material and the conductive sidewall spacer may be an edge or a portion of an edge of the conductive spacer. This is a very small area of contact. While not wishing to be bound by theory it is believed that reducing the size of the area of contact reduces the volume of the memory material which is programmed, thereby reducing the total current needed to program the memory device.

Hence, the use of a specially designed "multi-region" conductive sidewall spacer as an electrical contact as well as the unique positioning of the conductive spacer relative to the memory material provides for more efficient heating of the memory material as well as for more efficient use of the total energy supplied to the memory element. Hence, less total energy may be needed to affect a state change in the memory material (that is, less energy may be needed to program the device).

Hence, the multi-region conductive spacer provides a way to increase the flow of the heat energy into the memory material. In order to keep the heat energy within the memory material, a layer of insulation material (not shown)

may optionally be placed so that it at least partially surrounds the memory material. For example, referring to Figure 1D, a layer of insulation material may be disposed in between the memory material 290 and a portion of the second contact 300 to provide a "thermal blanket" for the memory material and serving to keep heat energy within the memory material layer 290.

An embodiment of a method for fabricating the memory device 100 from Figure 1D is shown in Figures 2A-2H. Referring first to Figure 2A, a substrate 102 is provided and a dielectric layer 128 is deposited on top of the substrate 102 to form the structure 200A shown in Figure 2A. The dielectric layer 128 may be a dielectric material such as silicon dioxide SiO_2 which may be deposited by means such as chemical vapor deposition (CVD).

Referring to Figure 2B, the dielectric layer 128 is then appropriately masked and etched to form the structure 200B having an opening 170 which preferably exposes a portion of the substrate 102. In the embodiment shown, the opening is formed as a trench. However, other embodiments are possible where the opening is formed as a hole (such as a circular or rectangular hole). The trench 170 which runs perpendicular to the plane of the illustration (that is, along the y-dimension). The trench 170 has sidewall surfaces 128S (corresponding to the sidewall surfaces of the dielectric regions 128) and bottom surface 106.

A layer 133 of a conductive material is deposited onto

the structure 200B to form the structure 200C shown in Figure 2C. Preferably, the deposition is a conformal deposition. The layer 133 is deposited onto the top surfaces 128T of the dielectric regions 128, onto the sidewall surfaces 128S of the dielectric regions 128, and onto the bottom surface 106 of the trench 170. Hence, portions of the layer 133 are deposited along the two sidewall surfaces 128S of the trench 170. These portions of the layer 133 are sidewall layer portions 133S of the layer 133. The conformal deposition of layer 133 may be done using chemical vapor deposition techniques. Other possible deposition methods may be used as long as the sidewall surfaces 128S are appropriately covered by the layer 133. The material of layer 133 will form the first region R1 of the conductive sidewall spacers 130A,B that are shown in Figure 1A. Hence, the material used for layer 133 is preferably a conductive material having the appropriate resistivity. Materials which may be used for layer 133 are those which are suitable for the first region R1. As noted above, these materials include n-type doped polysilicon, p-type doped polysilicon, n-type doped silicon carbide, p-type doped silicon carbide, titanium-tungsten, tungsten silicide, tungsten, molydenum, and titanium nitride. The n-type polysilicon may be formed "in situ" by depositing undoped polysilicon in the trench 170 using a CVD process in the presence of phosphene. Alternately, the n-type polysilicon may be formed by first depositing

undoped polysilicon and then doping the polysilicon with phosphorous or arsenic. P-type doped polysilicon may be formed by first depositing undoped polysilicon and then doping the polysilicon with boron.

After the layer 133 is conformally deposited it is then anisotropically etched. The anisotropic etch removes those sections of the layer 133 which are substantially horizontally disposed and leaves those sections which are substantially vertically disposed. Specifically, the anisotropic etch removes the substantially horizontally disposed sections of the layer 133 that were deposited on top surfaces 128T of the regions 128. It also removes the substantially horizontally disposed section of the layer 133 deposited onto the bottom surface 106 of trench 170. The anisotropic etch leaves those sections of the layer 133 conformally deposited along the sidewall surfaces 128S. Hence, the anisotropic etch leaves the sidewall layer portions 133S of the layer 133. The results of the anisotropic etch are shown as structure 200D in Figure 2D. The remaining sidewall layers 133S form the conductive sidewall spacers. At this point in the process, each of the conductive spacers comprises only the single sidewall layer 133S and each sidewall layer 133S comprises only a single region of material. In Figure 2D, the remaining sidewall layers 133S are shown as conductive sidewall spacers 130A,B.

Assuming that the layer 133 conformally coats the

surfaces onto which it is deposited, the conductive sidewall spacers 130A,B will have a lateral thickness substantially equal to the selected thickness of the layer 133. Preferably, the layer 133 is deposited so that the resulting conductive sidewall spacers 130A,B have a substantially uniform thickness between about 50 and about 1000 Angstroms, and more preferably between about 100 and about 500 Angstroms.

The conductive sidewall spacers 130A,B shown in Figure 2D extend continuously along the width of the trench 170 (i.e perpendicular to the plane of the illustration of Figure 2D). The next step in the process is to mask and etch the conductive sidewall spacers 130A,B so as to form a plurality of individual conductive sidewall spacers along the width of the memory array. These conductive spacers define individual memory elements along the channel width of the memory array.

The next step in the process is to fill the trench region 170 with a dielectric material such as silicon dioxide SiO_2. This may be done by depositing the dielectric material 140 onto the structure 200D to form structure 200E that is shown in Figure 2E. The dielectric material 140 is deposited into the trench 170 as well as onto the top surfaces of the dielectric regions 128. The deposition may be done using a chemical vapor deposition process. The structure 200E may then chemically mechanically polished (CMP) or dry etched to form the structure 200F shown in

Figure 2F. The chemical mechanical polishing or dry etching preferably planarizes the top surfaces of the conductive spacers to form top edges 132 which are substantially planar (as shown in Figure 2F).

The conductive sidewall spacers 130A,B shown in Figure 2F were formed by the deposition and anisotropic etch of a single layer of material (i.e., layer 133 shown in Figure 2C). Hence, each conductive spacer 130A,B shown in Figure 2F is a single sidewall layer comprising a single region of material. This region of material is denoted as the first region R1 in Figure 2F.

A second region R2 (as seen in Figure 1D), having a greater resistivity than region R1, may be formed in each of the conductive spacers 130A,B in several different ways. The approach used depends, at least in part, on the material of region R1. One way of forming the second region R2 is to alter a top portion of the region R1 of each conductive spacer 130A,B so as to increase the resistivity of the R1 material. "Top portion" refers to a section of the conductive sidewall spacer starting from the top edge 132 (or a portion of the top edge 132) and extending downwardly (i.e., toward the substrate) into the interior of the conductive sidewall spacer. Hence, a top portion of the conductive sidewall spacer includes all or a portion of the top edge 132 of the conductive spacer. Generally, any method of increasing the resistivity of the material is within the spirit and scope of this invention.

The resistance of the material may be increased using ion implantation techniques and/or by altering the dopant level of the material. For example, the second region R2 may be formed by appropriately "counter-doping" a top portion of the region R1 of each conductive spacer 130A,B shown in Figure 2F. In particular, if the regions R1 were formed from an n-type polysilicon, then a top portion of each region R1 may be counter-doped with boron (by well known ion implantation techniques) to form regions R2 having a resistivity which is greater than the resistivity of regions R1. If the n-type polysilicon of region R1 is lightly counter-doped with boron, then a region R2 may be formed which comprises n- polysilicon. If the n-type polysilicon of region R1 is more heavily counter-doped with boron, then a region R2 may be formed which comprises p- polysilicon.

Likewise, if the regions R1 were formed from a p-type polysilicon, then a top portion of each region R1 may be counter-doped with phosphorous to form regions R2 which also have a resistivity greater than the resistivity of regions R1. If the p-type polysilicon of region R1 is lightly counter-doped with phosphorous, then a region R2 may be formed which comprises p- polysilicon. If the p-type polysilicon of region R1 is more heavily counter-doped with phosphorous, than a region R2 may be formed which comprises n- polysilicon.

Hence, a top portion of the first region R1 may be

counter- doped to form a second region R2 which has a higher resistivity than the first region R1. A top portion of the region R1 may be sufficiently counter-doped with boron to form a second region R2 comprising n- polysilicon. Alternately, a top portion of the region R1 may be sufficiently counter-doped with boron to form a second region R2 comprising p- polysilicon. The multi-region conductive sidewall spacers 130A,B comprising a first region of material R1 and a second region of material R2 is shown in Figure 2G. The more resistive regions R2 start at the top edges 132. The height "h2" of the regions R2 are preferably less than about 1000 Angstroms, more preferably less than about 800 Angstroms, and most preferably less than about 600 Angstroms. The height of regions R1 is preferably less than about 10,000 Angstroms, more preferably, less than about 7,000 Angstroms, most preferably less than about 5,000 Angstroms. Of course, the heights of regions R1 and R2 may vary.

Referring now to Figure 2H, the structure 200H is formed by depositing a layer of memory material 290 on top of the structure shown in Figure 2G. A layer of conductive material 300 is then deposited on top of the memory layer 250 to form a second contact. It is noted that the deposited memory layer 290 is in contact with only each of the top edges 132 or a portion of each of the top edges 132 of the conductive spacers 130A,B. Substantially all electrical communication between each conductive spacer

132A,B and the memory material is through the edge 132 or a portion of the edge 132 of the respective conductive spacer.

It is noted that the multi-region conductive sidewall spacers may be made in another way. This is shown in Figures 2A'-2D'. The structure 200A' in Figure 2A' shows conductive sidewall spacers 130A,B comprising a single sidewall layer of material R1 (Figure 2A' is the same as Figure 2F). The structure 200A' may be masked and selectively etched to remove a top portion of the conductive sidewall spacers 130A,B so as to create recesses in a top portion of material R1 of each of the conductive spacers 130A,B. Referring to Figure 2B', the recesses 150 are shown in structure 200B'. The recesses 150 are filled by depositing a layer of material 160 on top of structure 200B' to form the structure 200C' shown in Figure 2C'. As shown in Figure 2C', the layer 160 fills the recesses 150 and also lies on top of the dielectric regions 128, 140. The structure 200C' may then be chemically mechanically polished (CMP) or dry etched to form the substantially planar top edges 132 as shown in structure 200D' of Figure 2D'. The structure 200D' includes conductive sidewall spacers 130A,B where each of the conductive spacers includes two regions of material - the first region R1 and the second region R2. The regions R2 consist of the material of layer 160 shown in Figure 2C'. It is noted that the structure shown in Figure 2D' is the same as the

structure shown in Figure 2G.

The second regions R2 shown in Figure 2D' may be formed of a material which, without any further modification, has the appropriate resistivity. As described above, examples of appropriate materials include n- doped polysilicon, p- doped polysilicon, n- doped silicon carbon compounds and/or alloys, p- doped silicon carbon compounds and/or alloys, titanium carbon-nitride, titanium aluminum nitride, titanium silicon-nitride, carbon, and forms of titanium nitride.

Preferably, the material chosen for the second region R2 has a resistivity that is greater than the resistivity of the R1 material removed by the etching process to create the recesses 150 (shown in Figure 2B').

Alternately, the second regions R2 may initially be formed of a material which still needs to be altered to increase its resistivity. For example, the regions R2 may initially be formed from an undoped polysilicon (that is, the layer 160 shown in Figure 2C' may be deposited as an undoped polysilicon). The undoped polysilicon of the second regions R2 may then be doped with boron to form a p- polysilicon region. Alternately, the undoped polysilicon of the second regions R2 may be doped with a material such as phosphorous or arsenic to form an n- polysilicon region. Hence, the resistivity may be increased by altering the dopant level of the material and/or by implanting ions into the material.

In the embodiment of the memory device shown in Figure 1A an electrical contact for each of the single-cell memory elements in the device is a conductive sidewall spacer. The conductive sidewall spacer 130A,B is a single sidewall layer formed along the sidewall surface of a trench by depositing a layer of conductive material into the trench and then anisotropically etching the layer to remove the horizontally disposed surfaces. The shape of the conductive spacer shown in Figures 1A and 1B are in the form of substantially planar sidewall layers.

Alternate forms of electrical contacts may be formed from sidewall layers that are made by the conformal deposition of material onto the other types of sidewall surfaces (that is, sidewall surfaces other that the sidewall surfaces of a trench). For example, a layer of conductive material may be substantially conformally deposited onto the surfaces of a hole (for example, a via), a mesa or pillar. The hole, mesa or pillar may be round, square, rectangular or irregularly shaped. Anisotropically etching the conformally deposited conductive layer, removes the horizontally disposed portions of the deposited layer and leaves only one or more vertically disposed portions. The remaining one or more vertically disposed portions are sidewall layers in the form of conductive sidewall spacers.

The sidewall spacer formed, for example, by the

conformal deposition of a conductive material into a cylindrical via hole (followed by an anisotropic etch) will be in the form of a cylindrical surface (with an axis substantially perpendicular to the substrate) having two open ends. Changing the shape of the hole, pillar or mesa will change the shape of the sidewall spacer. That is, the lateral cross section of the conductive sidewall spacer (i.e. the cross section parallel to the substrate) corresponds to the shape of the hole, mesa or pillar. It may be an annulus. Alternately, it may be rectangular or irregularly shaped. Figure 3A shows a three-dimensional view of a cylindrical, conductive sidewall spacer 330 formed in a circular via (and thus having a horizontal cross-section in the shape of an annulus). The cylindrical conductive spacer 330 is "single-layered". That is, it comprises a single, cylindrically shaped sidewall layer. The thickness "t" of this cylindrically shaped sidewall layer is the distance between the inner and outer cylindrical surfaces as shown in Figure 3A. The cylindrical sidewall layer has two open ends or "rims" forming the top edge 332 and the bottom edge 331. The top and bottom edges 332 and 331 of the cylindrically shaped conductive sidewall layer 330 are annular surfaces formed by intersecting the conductive layer 330 with a planes substantially parallel to the substrate. In the embodiment shown in Figure 3A, the layer of memory material 290 is adjacent only to the top end of the cylindrical sidewall

spacer 330. In particular, the memory material 290 is adjacent only to the top edge 332.

The layer 290 of memory material is deposited on top of the conductive spacer 330 and the second contact layer 300 is deposited on top of the memory material 290. The layer 290 of memory material (which is preferably substantially horizontally disposed) is adjacent only to the top edge 332 or portion of the top edge 332 of the conductive sidewall spacer 330 is adjacent to the memory material 290. All electrical communication between the conductive spacer 330 and the memory material 290 is through the top edge 332 or a portion of the top edge 332. Hence, area of contact between the conductive spacer 330 and the memory material 290 is the edge 332 or a portion of the edge 332. (That is, all or a portion of the annular surface 332).

Figure 3B is an example of a multi-regioned cylindrical conductive spacer 330. The conductive spacer 330 shown in Figure 3B comprises at least a first region R1 having a first resistivity and a second region R2 having a second resistivity. The resistivity of the second region R2 is greater than the resistivity of the first region R1. Preferably, the more resistive second region R2 is adjacent to the memory material while the less resistive first region R1 is remote to the memory material.

In the example shown in Figure 3B, the more resistive second region R2 is a "top portion" of the

conductive spacer adjacent to the top edge 332 (and remote to substrate 102). That is, it extends from the top edge 332 downwardly (i.e., toward the substrate 102) into the interior of the cylindrical conductive spacer for some distance "h2" (the "height" of the more resistive section region R2).

The regions R1 and R2 of the cylindrically shaped conductive spacer may be formed by methods similar to those used to form the regions R1 and R2 of the "planer" conductive spacer 130A,B shown in Figure 1A. The first region R1 and the second region R2 may be doped differently. For example, a more resistive second region R2 may be form by the appropriate ion-implantation techniques. Such ion implantation techniques may be used to appropriately counter-dope the material R1 to form the more resistive material R2. Alternately, the material R1 may first be etched and refilled with a more resistive material R2. Generally, all of the methods and materials described above (with respect to the planar conductive sidewall spacer) are applicable to this embodiment.

In the examples of the memory device shown in Figures 1A, 1D, 3A, and 3B the conductive sidewall spacer 130A,B (or 330) is adjacent to the memory material such that there are no "intermediate" layers disposed between the memory material and the conductive sidewall spacer 130A,B (or 330).

In an alternate embodiment of the present invention,

it is possible that one or more intermediate layers exit between the conductive sidewall spacer and the memory material. This is shown in Figure 1E, where an intermediate layer 280 is disposed between the memory layer 290 and the conductive sidewall spacer 130A,B. It is noted that, in this embodiment, it is still the case that substantially all electrical communication between the memory material 290 and the conductive sidewall spacer 130A,B is through the top edge 132 or a portion of top edge 132 of the conductive spacer 130A,B even though the layer 280 is disposed between the memory material 290 and the conductive spacer 130A,B. Furthermore, in the configuration shown in Figure 1E, the more resistive second region R2 is adjacent to the area of contact (which is top edge 132) while the less resistive first region R1 is remote to the area of contact (which is top edge 132). Also, it is seen that the more resistive second region R2 is positioned closer to the memory material 290 than the less resistive first region R1. That is, the second region R2 is "proximate to" the memory material while the first region R1 is "distant from" the memory material.

In yet another embodiment of the present invention, it is possible that the conductive sidewall spacers (such conductive spacers 130A,B in Figure 1D or conductive spacer 330 in Figure 3A) comprise one or more regions of material in addition to the more resistive second region R2 and the less resistive first region R1. In the embodiment shown in

Figure 1F, the conductive sidewall spacers 130A,B each comprise a third region R3 disposed between the memory material 290 and the second region R2. It is noted that in this embodiment, it is still the case that substantially all electrical communication between the memory material and the conductive sidewall spacer 130A,B is through the top edge 132 or a portion of the top edge 132. In the embodiment shown, the first and second regions R1 and R2 are positioned so that the region R2 is closer to the top edge 132 than region R1. (That is, region R2 is "proximate to" the top edge 132 while the region R1 is "distant from" to the top edge 132). Hence, region R2 is also closer to the area of contact between the conductive spacer and the memory material while the region R1 is further from the area of contact. (That is, region R2 is "proximate to" the area of contact while region R1 is "distant from" from the area of contact). Furthermore, it is also true that region R2 is closer to the memory material than region R1. (That is, region R2 is "proximate to" the memory material 290 while region R1 is "distant from" from the memory material).

In an alternate embodiment of the present invention, an electrical contact for a programmable resistance memory element may also be formed as a "conductive liner". The conductive liner is preferably a single layer of conductive material covering the sidewall surfaces as well as the

bottom surface of an opening such as a trench, hole or the like. Examples of conductive liners are shown in Figures 4A-C. In Figure 4A, the conductive liner 430A is formed in a trench. Figure 4B is an example of a conductive liner 430B formed in a rectangular hole. Figure 4C is an example of a conductive liner 430C formed in a circular hole. Of course, other shapes are also possible. As shown in the Figures 4A-4C, each conductive liner has one or more sidewall layer portions as well as a bottom layer portion. The top end of the conductive liners is an open end having a top edge 432. (In the specific examples shown, the "top edge" 432 of each conductive liner is the surface formed by intersecting the respective conductive liner with a plane substantially parallel with the substrate 102). It is noted that the U-shaped conductive liner shown in Figure 4A has a "dual" top edge 432.

It is noted that in the examples of the conductive liners shown in Figures 4A-4C, the sidewall layer portions are substantially vertically disposed. However, this does not have to be the case. The sidewall layer portions may be tilted. This would be the case if the conductive liners were formed in either a trench or via having angled sidewall surfaces.

The conductive liner is preferably edgewise adjacent to the memory material. That is, only an edge or a portion of an edge of the conductive liner is adjacent to the memory material. Substantially all of the remainder of the

conductive liner is remote to the memory material. Preferably, substantially all electrical communication between the conductive liner and the memory material is through an edge or a portion of an edge of the conductive liner (that is, through an "edge portion" of the conductive liner.

Figures 5A and 5B depicts an embodiment of the memory element of the present invention where one of the electrical contacts is a conductive liner 630 formed in a circular hole (for example, a via). Figure 5A is a three-dimensional view of the memory element. Figure 5B is a cross-sectional view parallel to the x-z plane.

As seen, the conductive liner 630 is a cylindrical shell having an open top end (remote to and facing away from the substrate 102) and a closed bottom end (proximate to the substrate). The open top end has an annular-shaped top edge 632. The conductive liner 630 is a cylindrically shaped sidewall layer portion 530S and a bottom layer portion 630B.

In the example shown in Figures 5A and 5B, the conductive liner 630 is in the shape of a cylindrically shaped cup. As shown in Figure 5B, the sidewall layer portion 630S forms the side of the cup while the bottom layer portion 630B forms the bottom of the cup. The top edge 632 may be referred to as the "rim" of the cup. The conductive liner may have other cup shapes such as a

paraboloid, hemisphere, cone, and frustum.

The layer 290 of memory material is preferably a planar, substantially horizontally disposed layer positioned adjacent to the open end of the conductive liner 630. Hence, the memory material is adjacent only to the top edge 632 (i.e., the rim) of the conductive liner 630 or a portion of the top edge 632 of the conductive liner. The remainder of the conductive liner 630 is remote to the memory material. Preferably, substantially all electrical communication between the conductive liner 630 and the memory material occurs through the edge 632 or a portion of the edge 632. Hence, the area of contact is defined by all or a portion of the edge 632 (i.e., an edge portion).

The edge 632 is an annulus having a thickness equal to the thickness of the conductive liner 630. The thickness of this annulus, and hence the area of contact between the conductive liner and the memory material may be reduced by decreasing the thickness of the conductive liner 630 deposited into the circular via hole.

The conductive liners may be formed so that they are "multi-regioned" and comprise at least a first region R1 having a first resistivity and a second region R2 having a second resistivity which is greater than the resistivity of the first region R1. This is shown in Figures 5C (a three-dimensional view) and in Figure 5D (a cross-sectional view parallel to the x-z plane). In the embodiment shown, the more resistive second region R2 is adjacent to the memory

material while the less resistive first region R1 is positioned remote to the memory material.

In the embodiment shown in Figures 5C and 5D, the more resistive region R2 is a "top portion" of the conductive liner adjacent to the top edge 632 and extending for some distance downwardly (toward the substrate) into the interior of the conductive liner. (That is, the more resistive top portion of the conductive liner includes all or a portion of the top edge 632).

It is noted that it is also possible that one or more intermediate layers be disposed between the memory material and the conductive liner. Also, it is possible that the conductive liner include at least a third region of material in addition to the first and second regions discussed above. The third region may be disposed between the memory material and the more resistive second region.

An embodiment of a method for fabricating the memory element 600 from Figures 5C and 5D is shown in Figures 6A-6F. Referring first to Figure 6A, a substrate 102 is provided and a dielectric layer 128 is deposited on top of the substrate 102. The dielectric layer may be formed from silicon dioxide and may be deposited by a chemical vapor deposition process. The dielectric layer 128 is then appropriately masked and etched to form a hole (for example, a via) 640 in the dielectric 128 as shown. The hole may be round, square, rectangular or irregularly shaped. In the embodiment shown in Figure 6A, the

resulting structure 600A is a circular via 640 which is formed in the dielectric 128. Figure 6B is a vertical cross-sectional view (parallel to the x-z plane) of the structure 600A shown in Figure 6A. The sidewall surface 128S and the bottom surface 106 of the cylindrical hole 640 is shown in Figure 6B.

A layer 633 of a conductive material is deposited on top of the structure shown in Figures 6A and 6B to form the structure 600C shown in Figure 6C. The layer 633 of conductive material is conformally deposited on top surfaces 128T of the dielectric region 128, on the sidewall surface 128S of the region 128 and the bottom surface 106 of the via hole 640. Hence, the layer 633 has a top portion 633T, a sidewall layer portion 633S, and a bottom layer portion 633B. It is noted that the layer 633 will form the first region R1 of the "dual-regioned" conductive liner electrical contact shown in Figures 5C and 5D. Hence, the materials chosen for the layer 633 should have the appropriate resistivity. The possible materials which may be used for the remote region R1 have been described above. As noted above, examples of appropriate materials which may be used for the first region R1 include n-type doped polysilicon, p-type doped polysilicon, n-type doped silicon carbide, p-type doped silicon carbide, titanium tungsten, tungsten silicide, tungsten, molybdenum, and titanium nitride. As discussed, a first region R1 of n-type polysilicon may be formed by depositing and doping

intrinsic polysilicon. That is, by doping intrinsic polysilicon in situ (i.e., CVD deposition in a phosphene environment). Alternately, n-type polysilicon may be formed by first depositing intrinsic polysilicon and then doping the polysilicon via ion implantation of phosphorous or arsenic. P-type polysilicon may be formed by first depositing intrinsic polysilicon and then doping the polysilicon via ion implantation of boron. Ion implantation may be performed by an "angle implant" whereby the ion beam comes in at an angle to an axis which is perpendicular to the substrate.

A layer of dielectric material 140 (such as silicon dioxide) may then be deposited on top of the layer 633 so as to fill the via 670 and form the structure 600D shown in Figure 6D. The structure 600D may then be chemically mechanically polished (CMP) or dry etched so as to planarize the top surface thereby removing the top surface 633T portion of the layer 633 and forming a cylindrical, cup-shaped conductive liner. This is shown as structure 600E in Figure 6E where the conductive liner 630 has a sidewall layer portion 630S along the sidewall 128S and a bottom layer portion 630B along the bottom surface 106. Furthermore, the conductive liner 630 has a top edge 632. Preferably, the planarization step forms a substantially planar top edge 632.

After this step in the process, the conductive liner 630 comprises only a single region of material which is

denoted in Figure 6E as the first region of material R1. The next step is to increase the resistivity of a portion of the conductive liner 630 that includes the top edge 632 or a portion of the top edge 632. As shown in Figure 6F, a second region R2, more resistive than the first region R1, is formed in a top portion of the conductive liner adjoining the edge 632. The second region R2 of the conductive liner may be formed by any of the methods which have been described above with regards to forming the multi-region conductive sidewall spacers. For example, the second region R2 may be formed by counter doping the n-type polysilicon of the first region R1. Specifically, the n-type polysilicon may be counter doped with boron to form a second region R2 comprising either n- or p- polysilicon. The second region may also be implanted with modifier elements in combination with the counter-doping ions or individually. Alternately, a top portion of the first region R1 may be removed (preferably, by being selectively etched) to form a recess. This recess may then be filled with a material which has a resistivity which is greater than the resistivity of the R1 material. For example, the recess may be filled with a material such as n- or p-polysilicon. Alternately, the recess may be filled with undoped polysilicon which can then be appropriately doped (preferably with boron, arsenic or phosphorus) to make it more resistive.

After the second region R2 is formed, the layer 290 of

memory material and the layer 300 of conductive material (forming the second electrical contact) may then be deposited. The area of contact between the conductive liner 630 and the memory material 290 is the surface portion of the conductive liner through which substantially all electrical communication (between the conductive liner and the memory material) occurs. This may be the entire edge 632 or a portion of the edge 632. (If the entire edge makes contact with the memory material then the area of contact is in the form of an annular ring). Hence, the memory material 290 is in electrical communication with the conductive liner 630 only through all or a portion of the edge 632.

Hence, one aspect of the present invention is a memory element comprising a programmable resistance memory element comprising a programmable resistance memory material and a means for delivering the electrical signal to the volume of memory material. Preferably, the means for delivering the electrical signal comprises a first and a second electrical contact (or electrode) where at least one of the electrical contacts is a multi-regioned contact comprising at least a first region R1 having a first resistivity and a second region R2 having a second resistivity greater than the resistivity of the first region R1. More preferably, the higher resistance second region R2 is adjacent to the memory material while the lower resistance first region R1 is remote to the memory material.

Generally, the multi-regioned contact may take any form. In the embodiments described above, the multi-regioned contact is in the form of a conductive spacer of liner which is edgewise adjacent to the memory material.

More generally, the multi-regioned electrode may be any layer of conductive material having any shape, conformation or physical geometry. In one embodiment, the contact layer may be positioned substantially perpendicular to the memory material. While not wishing to be bound by theory, it is believed that positioning the contact layer so that it is substantially perpendicular to the memory material may increase the effective amount of heat energy transferred to and remaining within the memory material. The area of contact (defined by the edge of the contact layer) is smaller when the contact layer is perpendicular to the memory material.

Also, it is believed that the less resistive material R1 (remote to the memory material) may behave as a heat sink, absorbing some of the heat generated by the more resistive portion R2 (adjacent the memory material). Positioning the contact layer substantially perpendicular to the memory material increases the average distance between the memory material and the less resistive material R1 of the contact layer. Hence, less of the Joule heat generated in or near the memory material is absorbed back by the contact layer.

Contact layers which are substantially vertically

disposed have been described above with reference to the conductive spacer and liners. As mentioned above, other embodiments of the substantially vertically disposed layers are possible which are not formed as conductive spacers or liners. That is, vertical layers may be formed without the conformal deposition of a layer onto a sidewall surface. For example, vertical layers may be formed with the use of oxide spacers.

The contact layer may also be substantially horizontally disposed. Figure 7A shows a three-dimensional view of an embodiment of a memory element 700 of the present invention formed on a substrate 102. The memory element 700 comprises the volume of memory material 750, a first electrical contact in the form of contact layer 730, and a second electrical contact 770 spacedly disposed from the contact layer 730. The contact layer 730 is a substantially horizontally disposed layer having an edge 732 adjacent to the memory material 750. Figure 7B is a vertical cross-sectional slice of the same memory device 700. The contact layer 730 has a first region R1 remote to the volume of memory material 750 and a second region R2 which is adjacent to the memory material 750. The adjacent second region R2 has a higher resistivity than the remote first region R1.

In the embodiment shown in Figures 7A,B the first contact 730 is a contact layer 730 which is substantially horizontally disposed onto the substrate 102. The contact

layer 730 is edgewise adjacent to the memory material 750. That is, the contact layer 730 has an edge 732 which is adjacent to the volume of memory material 750. The remainder of the contact layer 730 is remote to the memory material. Hence, all electrical communication between the contact layer 730 and the memory material 750 is through the edge 732. Hence, the area of contact between the memory material 750 and the contact layer 730 is the edge 732 of the contact layer 730. (As shown, in this embodiment the edge is a surface substantially parallel to the thickness of the contact layer). The area of contact between the contact layer 730 and the memory material 750 is proportional to the thickness of the contact layer 730.

Preferably, the edge 732 encircles a cross-sectional slice of the volume of memory material 750. As used herein, "encircles" means that the edge 732 passes completely around a cross-sectional slice of the volume of memory material 750. However, the memory element may be structured so that the edge only partially encircles a cross-sectional slice of the volume of memory material 750. In the embodiment shown, the cross-sectional slice is substantially parallel to the plane of the substrate 102, however, other orientations are also possible.

The second contact 770 may be a layer of conductive material and is preferably formed as a thin-film layer. In the embodiment shown in Figures 7A,B, the second contact

770 is a conductive layer deposited on top of the memory material 750 so that the bottom surface of the conductive layer 770 is adjacent to the top surface of memory material 750.

It is noted that one or more intermediate layers may be disposed between the memory material and the contact layer. Also, the contact layer may have one or more additional regions in addition to the first and second regions described above. It is possible that the additional regions be placed anywhere in the contact layer.

Another embodiment of the present invention is shown in Figure 8. Figure 8 shows a memory element 800 having a first contact 830 in electrical communication with memory material 850. Dielectric material 828 forms a trench or via structure. The first contact 830 includes a first region R1 having a first resistivity and a second region R2 having a second resistivity greater than the first resistivity. In the embodiment shown the first contact 830 is a single layer (that is, it is a single "contact layer"). The higher resistivity second region R2 is adjacent to the memory material while the lower resistivity first region is remote to the memory material. It is noted that in the embodiment shown in Figure 8, the electrical communication between the first contact 830 is through a portion of a face of the contact layer rather than through an edge of the contact layer. The first and second regions R1 and R2 may be formed from the appropriate contact materials.

Examples of appropriate materials have been described above. In one embodiment, the region R1 and the region R2 may be differently doped.

The memory element 800 also includes a second contact 870. In an alternate embodiment, the second contact 870 may also be multi-regioned. That is, it may also include at least a first region having a first resistivity and a second region having a second resistivity greater than the first resistivity.

As noted, in the embodiment shown in Figure 1A, substantially all electrical communication between the memory material 290 and conductive sidewall spacer 130A,B occurs through all or a portion of edge 132. Hence, the area of contact between the conductive spacer 130A,B and the memory material 290 is at least a portion of an edge the conductive sidewall spacer. The area of contact is thus very small and is proportional to the thickness of the conductive spacer adjacent to the memory material. Figures 1A and 1B are repeated as Figures 9A and 9B.

The area of contact may be reduced even further. In Figures 9A and 9B, each conductive sidewall spacer 130A,B has a substantially uniform width "w" (dimension of the spacer along the y-axis). In order to further decrease the area of contact between each conductive sidewall spacer 130A,B and the memory material, each conductive sidewall spacer may be formed so that its width is reduced (i.e.,

the conductive spacer is made narrower) adjacent to the memory material. Reducing the width "w" of the sidewall spacer adjacent the memory material reduces the area of contact between the conductive spacer and the memory material. This embodiment, referred to as a "rapier" design of the conductive spacer, is shown in Figure 9C. Figure 9C is a cross-sectional view of a memory device 100' using a conductive sidewall spacer 130'A,B with a rapier design. The plane of the illustration is parallel to the y-z plane. As shown, the top edge 132 of the conductive sidewall spacer has been appropriately etched so that its width w is reduced adjacent to the memory material. In particular, each conductive spacer has been appropriately recessed to form a protrusion or raised portion 135 adjacent to the memory material. The raised portion 135 extends from the recessed edge 132' and terminates at a distal end or top surface 137 adjacent the memory material 290. The top surface 137 of the raised portion 135 is also referred to as the "tip" or "peak" of the raised portion. Figure 9D is a idealized three-dimensional representation of the conductive spacers 130'A,B having raised portions 135 that extend from the edges 132'. The top surface or tip 137 of each of the raised portions has a thickness "t" and a width "w2". The thickness "t" is the thickness of the conductive layer 130'A,B adjacent to the memory material (not shown). Preferably, thickness "t" is less than about 750 Angstroms, more preferably less than about

500 Angstroms and most preferably less than about 300 Angstroms. The width "w2" of the raised portion 135 adjacent the memory material is less than the width "w1" of the sidewall layer 130'A,B adjacent the substrate 102. Preferably, the width "w2" is less than 700 Angstroms, more preferably less than 600 Angstroms and most preferably less than about 500 Angstroms. The thickness "t", the width "w2" as well as the surface area of the tip 137 may all be made smaller than what is permitted by photolithographic techniques. Preferably, the dimensions of the top surface 137 are sufficient so that the area of contact between the raised portion 135 and the memory material is preferably less than about 0.005 micron^2, more preferably less than about 0.0025 micron^2, and most preferably less than about 0.0015 micron^2.

The raised portion 135 may be made to have substantially vertical sidewalls (for example, substantially uniform width "w2" and substantially uniform thickness "t"), or it may be made to taper as it extends toward the tip 137 (for example, by tapering the width "w2 and/or by tapering the thickness "t"). Generally, the shape of the raised portion 137 is not limited to any particular shape. Examples of possible shapes include conical, pyramidal, prismatic and wedge-shaped frustums. The raised portion 137 may be columnar in form. The top surface or tip 137 of the raised portion 135 may be substantially flat or rounded. It is also conceivable that

the distal end or tip 137 may also be sharpened. The height of the raised portion 135 as well as the extent of any tapering may be controlled.

Referring again to Figure 1C, a dielectric material 145 is preferably positioned between the conductive sidewall layer 130'A,B and the memory material so that only the top surface 137 is exposed and in electrical contact with the memory material. Hence, substantially all electrical communication between each conductive layer 130'A,B and the memory material occurs through at least a portion of the top surface or tip 137 of the raised portion 135. The area of contact between each bottom electrode 130'A,B and the memory material is thus preferably defined by the top surface or tip 137. As noted above, in one embodiment of the invention it is preferable that the area of contact has an area less than about 0.005 micron^2, more preferably less than about 0.0025 micron^2, and most preferably less than about 0.0015 micron^2.

In an alternate embodiment of the invention, it is possible that the raised portion 135 be made to protrude into the memory material so that more of the surface of the raised portion 135 is in electrical contact with the memory material. It is noted that more than one raised portion may be formed on the edge 132' of each conductive layer 130'A,B.

The raised portions 135 may be made by forming a sidewall spacer over the conductive sidewall layers 130A,B

that are shown in Figure 1B. Specifically, the spacer is positioned above the conductive sidewall layers 130A,B where it is desired to position the raised portions 135. The spacer serves as a mask for either an anisotropic or isotropic etch. That is, the exposed sections of the edges 132 of the sidewall layers will be etched away and recessed while the section underlying the mask is at last partially protected from the etch so as to form raised portions or protrusions that extend from the recessed edges. Generally, the spacer which is used as the mask is not limited to any particular material. Preferably, the masking spacer is formed of a dielectric material such as an oxide or a nitride material. However, the masking spacer may also be formed of a semiconductor material such as a polysilicon. Moreover, it is also possible to form the masking spacer from a conductor such as aluminum. The spacer may be formed in many different ways.

An embodiment of a method for fabricating the memory device 100' of Figure 9C is shown in Figures 10A-10S. Referring first to Figure 10A, a substrate 102 is provided and a dielectric layer 128 is deposited on top of the substrate 102 to form the structure 1000A shown in Figure 10A. The dielectric layer 128 may be a dielectric material such as silicon dioxide SiO_2 which may be deposited by means such as chemical vapor deposition (CVD).

Referring to Figure 10B, the dielectric layer 128 is then appropriately masked and etched to form a window or

opening in the dielectric layer 128. The opening preferably exposes a portion of the substrate (and preferably the exposed portion of the substrate is a conductive portion of the substrate). In the embodiment shown in structure 1000B, the opening is a trench 170 which runs perpendicular to the plane of the illustration. The trench 170 has sidewall surfaces 128S (corresponding to the sidewall surfaces of the dielectric regions 128) and bottom surface 106.

A layer 133 of a conductive material is deposited onto the structure 1000B to form the structure 200C shown in Figure 10C. Preferably, the deposition is a substantially conformal deposition. The layer 133 is deposited onto the top surfaces 128T of the dielectric regions 128, onto the sidewall surfaces 128S of the dielectric regions 128, and onto the bottom surface 106 of the trench 170. Hence, portions of the layer 133 are deposited along the two sidewall surfaces 128S of the trench 170. These portions of the layer 133 are sidewall layer portions 133S of the layer 133. The conformal deposition of layer 133 may be done using chemical vapor deposition techniques. Other possible deposition methods may be used as long as the sidewall surfaces 128S are appropriately covered by the layer 133.

Generally, the material 133 may be any conductive material. For example, it may be a metal, a metal alloy or a doped polysilicon. Examples of materials which may be

used for layer 133 are include, but are not limited to, n-type doped polysilicon, p-type doped polysilicon, p-type doped silicon carbon alloys and/or compounds, n-type doped silicon carbon alloys and/or compounds, titanium-tungstem, tungsten, tungsten silicide, molybdenum, and titanium nitride. Other examples include titanium carbon-nitride, titanium aluminum-nitride, titanium silicon-nitride, and carbon.

The n-type polysilicon may be formed "in situ" by depositing polysilicon in the trench 170 using a CVD process in the presence of phosphene. Alternately, the n-type polysilicon may be formed by first depositing polysilicon and then doping the polysilicon with phosphorous or arsenic. P-type doped polysilicon may be formed by first depositing polysilicon and then doping the polysilicon with boron.

Preferably, the thickness of layer 133 is between about 50 and about 1000 Angstroms, and more preferably between about 100 and about 500 Angstroms.

After the layer 133 is conformally deposited it is then anisotropically etched. The anisotropic etch removes those sections of the layer 133 which are substantially horizontally disposed and leaves those sections which are substantially vertically disposed. Specifically, the anisotropic etch removes the substantially horizontally disposed sections of the layer 133 that were deposited on top surfaces 128T of the regions 128. It also removes the

substantially horizontally disposed section of the layer 133 deposited onto the bottom surface 106 of trench 170. The anisotropic etch leaves those sections of the layer 133 conformally deposited along the sidewall surfaces 128S. Hence, the anisotropic etch leaves the sidewall layer portions 133S of the layer 133. The results of the anisotropic etch are shown as structure 200D in Figure 10D. The sidewall layer portions 133S of layer 133 form the conductive sidewall spacers 130A,B. The sidewall spacers 130A,B are formed having the top edges 132.

The conductive sidewall spacers 130A,B shown in Figure 10D extend continuously along the y-axis dimension of the trench 170 (that is, perpendicular to the plane of the illustration of Figure 2D). The next step in the process is to mask and etch the conductive sidewall spacers 130A,B so as to form a plurality of individual conductive sidewall spacers along the y-axis dimension of the memory array. These conductive spacers define individual memory elements along the y-axis dimension of the memory array.

The dielectric material, such a silicon dioxide is then deposited into the opening 170 and onto the sidewall spacers 130A,B. The dielectric material preferably fills the opening 170. Referring to Figure 140, it is seen that the dielectric material 140 is preferably deposited into the trench 170 and on top of the dielectric layers 128 of structure 1000D to form structure 1000E. The deposition may be done using a chemical vapor deposition process. The

structure 1000E may then chemically mechanically polished (CMP) or dry etched to form the structure 1000F shown in Figure 10F. The chemical mechanical polishing or dry etching preferably planarizes the top surfaces of the sidewall layers 130A,B to expose at least a portion of one or both of the top edges 132. In the embodiment shown in Figure 10F, at least a portion of each of the edges 132 is exposed. A three dimensional representation of the structure 200F is shown in Figure 10F'.

A first oxide layer 240 (for example, silicon dioxide from a TEOS source) is deposited onto the top surface of structure 1000F to form the structure 1000G shown in the three-dimensional representation of Figure 10G. Figure 10G' is a cross-sectional view of the same structure 1000G parallel to the y-z plane and parallel to the width "w" of the sidewall spacer 130A,B. Preferably, the dimension of the first oxide layer 240 is between about 200 Angstroms and 500 Angstroms, and more preferably about 300 Angstroms. The first oxide layer 240 may be deposited using a chemical vapor deposition process. A layer 250 of polysilicon is then deposited on top of the oxide layer 240 to form structure 200H shown in the cross-sectional Figure 10H (parallel to the y-z plane) and in the three-dimensional representation of Figure 10H'. Preferably, the dimension of layer 250 is approximately 1000 Angstroms.

The structure 1000H is then appropriately masked and etch. A layer of photoresist material is applied on top of

the layer of polysilicon 250. The layer of photoresist is appropriately patterned (i.e., a pattern on a mask is transferred to the layer of photoresist) and a portion of the photoresist layer is removed to form the photoresist mask 260 shown in the three-dimensional view of Figure 10I. A top view of the structure 1000I parallel to the x-y plane is shown in Figure 10I'. Figure 10I' shows the relative positioning of the photoresist mask 260 relative to the top edges 132 of the conductive spacers 130A,B. A cross-sectional view of structure 1000I, parallel to the y-z plan, is shown in Figure 10I''.

The structure 1000I is then preferably dry etched to remove the portion of the polysilicon layer 250 which is not protected by the photoresist mask 260, thereby forming the structure 1000J shown in Figure 10J. The etch used is selective to the oxide layer 240. The etch forms a sidewall surface 252 in the polysilicon layer 250. The photoresist 260 is then stripped from structure 1000J to form structure 1000K shown in Figure 10K.

A second oxide layer 270 (such as silicon dioxide) is then deposited onto the structure 1000K to form the structure 1000L shown in Figure 10L. Preferably, the layer 270 is deposited to a thickness of about 600 Angstroms. The second oxide layer 270 is deposited onto top horizontal surface of the polysilicon layer 250 as well as onto the exposed portion of the first oxide layer 240. It is also deposited along the sidewall surface 252 of the polysilicon

layer 250. The oxide layer 270 is then anisotropically etched to remove the horizontally disposed portions of second oxide layer 270 and leave the vertically disposed portion 270A along the sidewall surface 252. The resulting structure is shown as structure 1000M in Figure 10M. The remaining portion the oxide layer 270 is the portion 270A. The portion 270A is a sidewall spacer.

The remaining portion of the polysilicon layer 250 shown in Figure 1000M is then removed. This is preferably done by using a polysilicon dry etch. It is possible to use a wet polysilicon etch as well. The resulting structure is shown as structure 1000N in Figure 10N. After this, the structure 1000N is subjected to an anisotropic etch to remove the portions of the first oxide layer 240 that are not covered by the spacer 270A, leaving the oxide spacer 270B as shown by structure 1000 O in Figure 10 O. A three dimensional representation of the structure 1000 O is shown in Figure 10 O'. A top view (parallel to the x-y plane) of the oxide spacer 270B and its positioning relative to the top surfaces 132 of the conductive layers 130A,B is shown in Figure 10 O''. As seen, the spacer 270B overlies a portion of each of the exposed edges 132 of the sidewall spacers 130A,B. The "thickness" of the oxide spacer 270B (i.e. the spacer's lateral dimension in the y-axis dimension) is preferably smaller than which could be achieved though photolithographic methods (i.e., smaller than a photolithographic limit). In one embodiment, the

thickness dimension of the oxide spacer 270B is preferably less 1000 Angstoms. In another embodiment, the thickness of the oxide spacer is preferably less than 700 Angstroms, more preferably less than 600 Angstroms and most preferably less than about 500 Angstroms.

Using the oxide spacer 270B as a mask, the conductive layers are then etched to remove a portion of the conductive layers 130A,B and form raised portions underneath the spacer 270B. Referring to Figure 10P, at least a portion of each of the conductive layers not covered by the oxide spacer 270B is etched away and removed to form the recessed edges 132. However, at least a portion of each of the conductive layers covered by the oxide spacer 270B is at least partially protected from the etch to form the raised portions 135 that extend upwardly from the recessed edges. Figure 10P' is a cross-section view through a recessed conductive layer 130'A,B parallel to the y-z plane. The etch used may, for example, be a wet etch or a dry etch. Preferably, the etch used is a dry etch such as a plasma etch. The etch is preferably anisotropic so as to form raised portions 135 having substantially straight sidewalls. However, an isotropic etch may be used which removes a portion of the conductive material underneath the spacer and forms raised portions with sloped or tapered sidewalls. Hence, the raised portions 135 may be tapered (where the degree of tapering is controlled by the etching process used). Preferably,

the raised portions 135 may have a height of about 500 Angstroms to about 2500 angstroms.

A layer 145 of a dielectric material (such as silicon dioxide) is then deposited onto the top of the structure 200P preferably by using conventional deposition methods (such as chemical vapor deposition) to form the structure 1000Q shown in Figure 10Q. The material is deposited into the recesses 138, onto the recessed edges and at least partially over the raised portions. The dielectric layer 145 and the oxide spacer 270B may then be chemically mechanically polished (CMP) to expose at least a portion of the top surface or tip 137 of each of the raised portions 135 and form the structure 1000R shown in Figure 10R. (Of course, it may be possible to expose at least a portion of just one of the tips 137). A layer of memory material 290 and a second electrical contact 300 (i.e., a top electrode) are deposited on top of the structure shown in Figure 10R to form the memory element shown in Figure 10S.

It is noted that, after chemical mechanical polishing to form the structure 200R shown in Figure 10R (and before the deposition of the memory material), a barrier layer may, optionally, be formed on top of the structure 1000R. (Hence, the barrier material would be formed between the tip (or top surface) 137 of the raised portion and the memory material). Barrier layer materials may be chosen to increase the conductivity between the electrical contact and the memory material, and/or improve the adhesion

between the electrical contact and the memory material, and/or to prevent the electromigration of the electrical contact material into the memory material. Examples of certain barrier layer materials include, but are not limited to, titanium silicide, cobalt silicide and tungsten silicide.

Referring again to Figures 10P and 10P', it is again noted that etching the conductive sidewall layers forms the narrow recesses 138 where the conductive layers are not underlying the oxide spacer 270B. After etching the conductive layers to form the recesses, it may be desirable to then etch the surrounding oxide regions 128 and 140 to the same level as the recessed edges 132' prior to depositing the dielectric layer 145 (as shown in Figure 2Q). This would eliminate the need for the dielectric material 145 to fill the narrow recesses 138. This would also make the subsequent chemical mechanical processing step (to get to the structure shown in Figure 10R) easier.

As shown above, the raised portions 135 may be made with the use of oxide spacers. As noted above, other materials may be used to form the spacers. In another embodiment of the present invention, the raised portions may be also made with nitride spacers that are preferably formed from silicon nitride. Referring Figures 10G through 10L, nitride spacers may be formed by replacing the first oxide layer 240 with a first silicon nitride layer, by replacing the polysilicon layer 250 with an oxide layer

(such as silicon dioxide from a TEOS source) and by replacing the second oxide layer 270 with a second silicon nitride layer. The polysilicon etch (used to etch the polysilicon 250 as shown in Figures 10J and 10N) would be replaced with an oxide etch selective to an underlying silicon nitride material. Likewise, the oxide etch (used to anisotropically etch the oxide layers as shown in Figures 10M and 10 O) would be replaced with a silicon nitride etch.

More generally, the disclosed technique for forming raised portions above a conductive material should not be limited to the embodiments disclosed herein. The spacers may be formed using many different techniques. Also, the spacers may be formed from many different materials including dielectrics (for example, oxide and nitride), semiconductor materials (such as polysilicon) and conductors (such as aluminum). Likewise, the materials chosen for the layers 240, 250, 260 and 270 (as shown in the processing steps of Figures 10G through 10 O) are not limited to the embodiments provided and a wide range of materials may be used for each of the layers. The particular materials selected for each of the layers are preferably chosen to provide the proper selectivity during the various etching processes as will be recognized by persons of ordinary skill in the art.

As noted, the raised portions or protrusions as well the remaining conductive layer may be formed from any

conductive material. Examples of materials include, but are not limited to, n-type doped polysilicon, p-type doped polysilicon, p-type doped silicon carbon alloys and/or compounds, n-type doped silicon carbon alloys and/or compounds, titanium-tungstem, tungsten, tungsten silicide, molybdenum, and titanium nitride. Other examples include titanium carbon-nitride, titanium aluminum-nitride, titanium silicon-nitride, and carbon.

Referring now to Figure 11, it is seen that the electrode structure having a raised portion 135 may be formed to have a first portion R1 and a second portion R2 having a resistivity which is greater than the resistivity of the first portion R1. As shown the more resistive second portion R2 is adjacent to the memory material while the less resistive first portion R1 is remote to the memory material.

In the embodiment of the memory device shown in Figure 10S, the raised portion 135 extends from an edge of conductive layer 130'A,B. In the example shown, the conductive layer is a substantially planer, sidewall layer formed along the sidewall surface of a trench by depositing a layer of conductive material into the trench and then anisotropically etching the layer to remove the horizontally disposed surfaces.

More generally, raised portions may be formed on any conductive material having any physical geometry. In particular, in particular, raised portions or protrusions

may be formed on an edge of any conductive layer (such as an conductive sidewall) having any physical geometry. Alternate forms of conductive sidewall layers may be made by the conformal deposition of a conductive material onto sidewall surfaces having various shapes and configurations. For example, a layer of conductive material may be substantially conformally deposited onto the sidewall surfaces of an opening (such as a via), a mesa or a pillar. The opening, mesa or pillar may be round, square, rectangular or irregularly shaped (likewise, the opening may be a trench). Anisotropically etching the conformally deposited conductive layer, removes the horizontally disposed portions of the deposited layer and leaves only one or more vertically disposed portions. The remaining one or more vertically disposed portions are sidewall layers in the form of conductive sidewall spacers having different shapes.

Figure 12A is the three-dimensional view of the cylindrical conductive sidewall spacer 330 from Figure 3A. The spacer 330 is formed in a circular opening (and thus having a horizontal cross-section in the shape of an annulus).

The raised portions or protrusions may be formed atop the annular edge of a cylindrical sidewall layer. Figure 12B is a three-dimensional representation of a cylindrical conductive sidewall layer 330′ that includes raised portion or protrusions 335 that extend from the edge 332′. Each

raised portion 335 extends from edge 332' to an end or tip 337 adjacent the memory material (not shown). As noted above, the raised portions 335 are not limited to any particular shape. In the embodiment shown, the raised portions 335 have a thickness "t" (proportional to the thickness of the conductive layer) and a width "w". Conductive layer 330' is in the form of a cylindrical conductive spacer. The raised portions may be formed on the top edge of the cylindrical conductive layer 330' with the use of oxide spacers or nitride spacers as described above. An example of forming the raised portions atop the annular edge of a cylindrical sidewall layer will be given below. Preferably, substantially all electrical communication between the conductive spacer 330' and the memory material is through one or more of the raised portions 335. More preferably, substantially all electrical communication between the conductive spacer 330' and the memory material is through the upper surface or tip 337 of one or more of the raised portions 335. The electrical contact 330' and memory material may be positioned so that only all or a portion of the top end or tip 337 of one or more of the raised portions 335 are adjacent to the memory material while substantially all of the remaining portion of the electrical contact is remote to the memory material.

Figure 12C is a two dimensional side view of the cylindrical conductive layer 330', parallel to the x-z

plane, showing the memory material 290 as well as the top electrical contact 300 (and also insulation materials 128, 140 and 180). In Figure 12C both of the raised portions 335 are in electrical communication with the memory material. However, it is also possible that the memory material and the raised portions 335 and the memory material be positioned relative to each other so that only one of the protrusions 335 is touching the memory material. In the embodiment shown in Figure 12C only the top surfaces or tips 337 are adjacent the memory material while the remainder of the electrical contact is remote to the memory material.

Raised portions may also be formed on conductive liners such as the conductive liners shown in Figures 4A through 4C.

Figures 5A and 5B depict an embodiment of the memory element where the bottom electrical contact is a conductive liner 630 formed in a circular opening. Figures 13A and 13B is the conductive liner from Figures 5A and 5B. Figure 13A is a three-dimensional view of the memory element while Figure 13B is a cross-sectional view parallel to the x-z plane.

As noted, one or more raised portions or protrusions may be formed on the top edge of the sidewall portion of a conductive liner. Figure 13C shows the cylindrical conductive liner 630′ disposed on top of a substrate 102. In this embodiment, the conductive liner 630′ includes at

least one raised portion or protrusion 635. Each of the raised portions extends from the top edge 632' to a distal end or tip 637 (also referred to as a top surface) adjacent the memory material (the memory material is not shown in this diagram). In the embodiment shown, the raised portions 635 each have a thickness "t" (which is substantially the same as the thickness of the remainder of the conductive liner 630') and a width "w". Preferably, substantially all electrical communication between the conductive sidewall spacer 630' and the memory material is through one or more of the raised portions 635. More preferably, substantially all electrical communication between the conductive spacer 630' and the memory material occurs through the top surface or tip 635 of one or more of the raised portions 635. Hence, the electrical contact 630' and memory material may be positioned so that only the top surface 637 of one or more of the raised portions 635 is adjacent to the memory material while substantially all of the remaining portion of the electrical contact is remote to the memory material.

Figure 13D shows a side view of a memory element, parallel to the x-z plane, made using the conductive liner 630'. Shown are memory material 290 and second electrical contact 300. In Figure 13D, the tips 637 of both protrusions 635 are in electrical contact with the memory material; however, it is possible that the memory material be positioned so that it is in electrical contact with only

the upper surface 637 of only one of the protrusions 635. The base of the conductive liner 630' is adjacent to and in electrical communication with the substrate 102.

The raised portions 635 may be formed with the use of sidewall spacers as described above. The sidewall spacers may be formed, for example, of oxide or silicon nitride. An embodiment of a method for fabricating the conductive liner 630' is shown Figures 14A-14S'. Referring first to Figure 14A, a substrate 102 is provided and a dielectric layer 128 is deposited on top of the substrate 102. The dielectric layer may be formed from silicon dioxide and may be deposited by a chemical vapor deposition process. The dielectric layer 128 is then appropriately masked and etched to form a window or opening in the form of opening 610 in the dielectric 128 as shown. The opening may be round, square, rectangular or irregularly shaped. Alternately, the dielectric layer 128 may be masked and etched to form a trench. Preferably, the opening (or trench) is made through the dielectric layer 128 to the substrate 102. In the embodiment shown in Figure 14A, the resulting structure 1400A is a circular opening 610 which is formed in the dielectric 128. Figure 14B is a cross-sectional view (parallel to the y-z plane) of the three-dimensional structure 1400A shown in Figure 14A. The sidewall surface 128S and the bottom surface 106 of the circular opening 610 is shown in Figure 14B. Preferably, the opening exposes at least a portion of the substrate.

A layer 633 of a conductive material is deposited on top of the structure shown in Figures 14A and 14B to form the structure 600C shown in Figure 14C. The layer 633 of conductive material is conformally deposited on top surfaces 128T of the dielectric region 128, on the sidewall surface 128S of the region 128 and the bottom surface 106 of the opening 640. Hence, the layer 633 has a top portion 633T, a sidewall layer portion 633S, and a bottom layer portion 633B.

A layer of dielectric material 140 (such as silicon dioxide) may then be deposited on top of the layer 633 so as to preferably fill the opening 610 and form the structure 1400D shown in Figure 14D. The structure 1400D may then be chemically mechanically polished (CMP) or dry etched so as to planarize the top surface thereby removing a portion of layer 140 as well as the top layer portion 633T of the layer 633. The etch forms a cylindrical, cup-shaped conductive liner 630 having a sidewall layer portion 630S along the sidewall 128S and a bottom layer portion 630B along the bottom surface 106 as shown in Figure 14E. The etch also forms the edge 632. In the embodiment shown the edge 632 has the shape of an annulus. Preferably, the planarization step forms an edge which is substantially planar. Figure E' shows a three-dimensional representation of the structure 1400E from Figure 14E.

One or more raised portions or protrusions may be formed atop the edge 632. The processing steps for forming

raised portions that extend from the top edge of the conductive liner are the similar to those described above with respect to the conductive sidewall spacers. A first oxide layer 640 is deposited on top of the conductive liner 600E to form the structure 1400F shown in the three-dimensional representation of Figure 14F and in the cross-sectional view (parallel to the y-z plane) of Figure 14F'. A polysilicon layer 650 is deposited onto the first oxide layer 640 so form structure 1400G as shown in Figures 14G and 14G'. A photoresist resist layer is deposited onto the polysilicon layer 650 and appropriately patterned to form photoresist mask 660 as shown in Figure 14H. A top view (parallel to the x-y plane) of the positioning of the photoresist layer 660 relative to the annular edge of the conductive cup 630 is shown in Figure 14H'. A cross-sectional view (parallel to the y-z plane) is shown in Figure 14H''. The polysilicon layer 650 is appropriately patterned and etched to form a sidewall surface 652 in the layer 650 as shown in structure 1400I of Figure 14I. The photoresist material is then removed as shown in Figure 14J. A second oxide layer 670 is conformally deposited over the top surface and the sidewall surface 652 of the remaining portion of the polysilicon layer 650 as well as over the top surface of the first oxide layer 640 as shown in Figure 14K. The horizontally disposed portions of the second oxide layer 670 are then removed preferably by an anisotropic etch of the oxide layer 670 leaving the

vertically disposed oxide portion 670A along the sidewall surface of the polysilicon layer 650 as shown in Figure 14L. The remaining portion of the polysilicon layer 650 is then removed as shown in Figure 14M. The remaining oxide layer 640 and oxide portion 6A are then anisotropically etched to remove that portion of the oxide layer 640 that is not covered by the oxide spacer 670A. The remaining portion is the oxide spacer 670B shown in Figures 14N (parallel to the y-z plane) and 14N′ (a three-dimensional view). Figure 14N′′ is a top view parallel to the x-y plane of the structure 600N. As shown in Figure 14N′′, the oxide spacer 670B is overlying a portion of the edge 632.

Using the oxide spacer 670B as a mask, the conductive layer 630 is then etched to form one or more raised portions underneath the spacer. Referring to Figure 14 O, at least a portion of the conductive layer not covered by the spacer is etched away and removed to form a recessed edge 632′. However, at least a portion of the conductive layer covered by the oxide spacer 670B is at least partially protected from the etch to form the raised portions 635 that extend upwardly from the recessed edge. A side view (parallel to the y-z plane) of an etched conductive cup 630′ having recessed edge 632′ and raised portions 635 is shown in Figure 6P. Recession 638 is the gap formed between the oxide materials 128, 140 as a result of etching the conductive liner 630. As noted above, the etch may be anisotropic or isotropic. As well, the etch

may be a dry etch or a wet etch.

An oxide layer 680 is then deposited into the recession 638 and on top of dielectric layers 128 and 140 as shown (as a cross-sectional view parallel to the y-z plane) in Figure 14Q. The oxide layer 680 and the oxide spacer 670B may then be chemically mechanically polished to expose at least a portion of the top surfaces or tips 637 of the raised portions 635 and to form structure 1400R as shown in Figure 14R. A layer of programmable resistance memory material is disposed adjacent at least a portion of the raised portions. Referring to Figure 14S, a layer of memory material 690 is deposited on top of the structure 1400R and, in particular, over at least a portion of one or both of the tips 627. A conductive layer 695 is deposited over the memory material 690 to form the upper electrode of the memory element 1400S as shown in Figure 14S (a side view parallel to the y-z plane). Figure 14S' shows an alternate side view of the structure 600S parallel to the x-z plane that shows the conductive liner 630' and both of the raised portions 635 with tips 637 adjacent the memory material 690. Only the top surfaces 637 of the raised portions 635 are adjacent to the memory material 690 while the remainder of the raised portions as well as the remainder of the conductive liner 630' is remote to the memory material 690. It is noted that the memory layer 690 may be positioned to that it is adjacent to only one of the raised portions 635.

It is noted, prior to the deposition of the oxide layer 680 shown in Figure 14Q it is possible to etch the dielectric regions 128 and 140 (shown in Figure 14P) to the level of the recessed edge 632'. This avoids the need to have the oxide material 680 fill the narrow gap 638 and also facilitates the chemical mechanical polishing. Also, as discussed above, it is possible to form protrusions 635 by using spacers formed from other dielectrics such as silicon nitride. Moreover, it is also possible to form spacers from semiconductor materials such as polysilicon or from conductors such as aluminum.

It is noted that in the embodiment of the method for forming the raised portion disclosed above, a sidewall spacer is used as a mask and a portion of the conductive material that does not underlie the mask (the sidewall spacer) is removed to form the raised portion. It is also possible that other types of masks may be used which are not sidewall spacers. For example different types of patterned layers may be used as masks to form the raised portions. For example, it is possible that the patterned layers may simply be a portion of a layer (such as an oxide, nitride or polysilicon layer) which is formed on a portion of the edge of the conductive layer. Alternately, it is possible that the mask be a thin vertically disposed strip which is not formed as a sidewall layer.

A lateral dimension of the mask is a dimension of the mask as measured parallel to the substrate. For example, a

lateral dimension may, for example, be the dimension of the mask as measured along either the x-axis or the y-axis when the substrate is parallel to the x-y plane. Preferably, at least one of the lateral dimensions of the mask is less than that which could be achieved through photolithography (i.e., it is less than a photolithographic limit). In one embodiment, at least one of the lateral dimensions is preferably less than about 1000 Angstroms. In another embodiment, at least one of the lateral dimensions is less than about 700 Angstroms, more preferably less than about 600 Angstroms, and most preferably less than about 500 Angstroms.

Likewise, other methods, besides the one presented above, may be used to form the masking sidewall spacers that are used to form the raised portions on the conductive materials. The methods and materials used depend, of course, on the underlying conductive material. For example, in an alternate method, a layer of polysilicon (a first layer) is deposited over the conductive material. The layer of polysilicon is then be patterned and etched to form a sidewall surface. An oxide layer (a second layer) is then deposited onto the sidewall surface of the polysilicon. The oxide layer is anisotropically etched to remove the horizontally disposed surfaces and leave the sidewall spacer on the polysilicon. The polysilicon is then removed to leave only the oxide sidewall spacer that can now be used as mask. As described above, a portion of

the conductive material not covered by the spacer is etched so as to form a raised portion extending from the conductive material under the spacer. The polysilicon and the oxide may, of course, be replaced with other materials. The materials chosen for the different layers (i.e., the first and second layers) depend upon the underlying conductive material and also upon the appropriate selectivity during the various etching processes. Still other methods known in the art may be used to form the masking spacers.

The raised portions or protrusions may be formed on an edge of the sidewall layers of different conductive liners. For example, they may be formed on the conductive liners shown in Figures 4A-4C. Figure 7 provides an example of a U-shaped conductive liner 720 that is formed in a trench. Figure 7 shows conductive liner 720 having two sidewall layer portions 730 and a bottom layer portion 740. The raised portions or protrusions 735 are formed on the edges 732 of the two sidewall layer portions 730 of the conductive liner 720. The protrusions 735 extend from the edges 732 to tips 737. Substantially all of the electrical communication between the conductive liner 720 and the memory material (not shown) is preferably through one or both of the raised portions 735, and more preferably, through one or both of the top surfaces 737.

Hence, as disclosed above raised portions or protrusions may be formed on an edge of a conductive

sidewall layer to form novel electrical contact structures. More generally, raised portions may be formed on the edge of any conductive layer having any shape or orientation. Still, more generally, one or more raised portions may be formed on any conductive material having any physical geometry.

As noted above, to increase the amount of heat energy transferred into the memory material, it may be possible to increase the resistivity of the top surface or tip of the raised portion or protrusion that extends from the edge of the electrical contact. An example of this type of structure is shown in Figure 11 above.

The memory elements of the present invention may be electrically coupled to isolation/selection devices and to addressing lines in order to form a memory array. The isolation/addressing devices permit each discrete memory cell to be read and written to without interfering with information stored in adjacent or remote memory cells of the array. Generally, the present invention is not limited to the use of any specific type of isolation/addressing device. Examples of isolation/addressing devices include field-effect transistors, bipolar junction transistors, and diodes. Examples of field-effect transistors include JFET and MOSFET. Examples of MOSFET include NMOS transistors and PMOS transistors. Furthermore NMOS and PMOS may even be formed on the same chip for CMOS technologies.

Hence, associated with each memory element of a memory array structure is isolation/addressing device which serves as an isolation/addressing device for that memory element thereby enabling that cell to be read and written without interfering with information stored in other adjacent or remote memory elements of the array.

The memory element of the present invention comprises a volume of memory material. Generally, the volume of memory material is a programmable resistance memory material which is programmable to at least a first resistance state and a second resistance state. The memory material is preferably programmed in response to electrical signals. Preferably, the electrical signals used to program the materials are electrical currents which are directed to the memory material.

In one embodiment, the memory material is programmable to two resistance states so that each of the memory elements is capable of storing a single bit of information. In another embodiment, the memory material is programmable to at least three resistance states so that each of the memory elements is capable of storing more than one bit of information. In yet another embodiment, the memory material is programmable to at least four resistance states so that each of the memory elements is capable of storing at least two bits of information. Hence, the memory materials may have a range of resistance values providing for the gray scale storage of multiple bits of information.

The memory materials may be directly overwritable so that they can be programmed from any of their resistance states to any other of their resistance states without first having to be set to a starting state. Preferably, the same programming pulse or pulses may be used to program the memory material to a specific resistance state regardless of its previous resistance state. (For example, the same current pulse or pulses may be used to program the material to its high resistance state regardless of its previous state). An example of a method of programming the memory element is provided in U.S. Patent No. 6,075,719, the disclosure of which is incorporated by reference herein.

The memory material may be a phase change material. The phase-change materials may be any phase change memory material known in the art. Preferably, the phase change materials are capable of exhibiting a first order phase transition. Examples of materials are described in U.S. Patent Nos. 5,166,758, 5,296,716, 5,414,271, 5,359,205, 5,341,328, 5,536,947, 5,534,712, 5,687,112, and 5,825,046 the disclosures of which are all incorporated by reference herein.

The phase change materials may be formed from a plurality of atomic elements. Preferably, the memory material includes at least one chalcogen element. The chalcogen element may be chosen from the group consisting

of Te, Se, and mixtures or alloys thereof. The memory material may further include at least one element selected from the group consisting of Ge, Sb, Bi, Pb, Sn, As, S, Si, P, O, and mixtures or alloys thereof. In one embodiment, the memory material comprises the elements Te, Ge and Sb. In another embodiment, the memory material consists essentially of Te, Ge and Sb. An example of a memory material which may be used is $Te_2Ge_2Sb_5$.

The memory material may include at least one transition metal element. The term "transition metal" as used herein includes elements 21 to 30, 39 to 48, 57 and 72 to 80. Preferably, the one or more transition metal elements are selected from the group consisting of Cr, Fe, Ni, Nb, Pd, Pt and mixtures or alloys thereof. The memory materials which include transition metals may be elementally modified forms of the memory materials in the Te-Ge-Sb ternary system. This elemental modification may be achieved by the incorporation of transition metals into the basic Te-Ge-Sb ternary system, with or without an additional chalcogen element, such as Se.

A first example of an elementally modified memory material is a phase-change memory material which includes Te, Ge, Sb and a transition metal, in the ratio $(Te_aGe_bSb_{100-(a+b)})_cTM_{100-c}$ where the subscripts are in atomic percentages which total 100% of the constituent elements, wherein TM is one or more transition metals, a and b are as set forth herein above for the basic Te--Ge--Sb ternary system and c

is between about 90% and about 99.99%. Preferably, the transition metal may include Cr, Fe, Ni, Nb, Pd, Pt and mixtures or alloys thereof.

A second example of an elementally modified memory material is a phase-change memory material which includes Te, Ge, Sb, Se and a transition metal, in the ratio $(Te_aGe_bSb_{100-(a+b)})_cTM_dSe_{100-(c+d)}$ where the subscripts are in atomic percentages which total 100% of the constituent elements, TM is one or more transition metals, a and b are as set forth hereinabove for the basic Te-Ge-Sb ternary system, c is between about 90% and 99.5% and d is between about 0.01% and 10%. Preferably, the transition metal may include Cr, Fe, Ni, Pd, Pt, Nb, and mixtures or alloys thereof.

It is to be understood that the disclosure set forth herein is presented in the form of detailed embodiments described for the purpose of making a full and complete disclosure of the present invention, and that such details are not to be interpreted as limiting the true scope of this invention as set forth and defined in the appended claims.

It is to be understood that the disclosure set forth herein is presented in the form of detailed embodiments described for the purpose of making a full and complete disclosure of the present invention, and that such details are not to be interpreted as limiting the true scope of

this invention as set forth and defined in the appended claims.

We claim:

1. An electrically operated memory element, comprising:

a volume of memory material programmable to at least a first resistance state and a second resistance state; and

an electrical contact in electrical communication with said memory material, said conductive sidewall spacer including at least a first region having a first resistivity and a second region having a second resistivity greater than said first resistivity.

2. The memory element of claim 1, wherein said second region is adjacent said memory material.

3. The memory element of claim 1, wherein said electrical contact is a conductive layer.

4. The memory element of claim 1, wherein said electrical contact is a conductive sidewall liner or conductive sidewall spacer.

5. The memory element of claim 1, where said electrical contact is edgewise adjacent said memory material.

6. The memory element of claim 1, wherein substantially all of said electrical communication is through at least a portion of an edge of said electrical contact.

6. The memory element of claim 1, wherein said first region and said second region are differently doped.

7. The memory element of claim 1, wherein said electrical contact includes a raised portion extending to a distal end adjacent said memory material.

8. The memory element of claim 1, wherein said memory material is a phase change material.

9. A method of making an electrically operated memory element, comprising the steps of:

providing a conductive material;

increasing the resistivity of a portion of said conductive material; and

depositing a memory material adjacent said portion.

10. The method of claim 9, wherein said increasing the resistivity step comprising the step of altering the dopant level of said portion.

11. The method of claim 9, wherein said increasing the resistivity step comprises the step of implanting ions into said layer portion.

12. The method of claim 9, wherein said increasing the resistivity step comprises the steps of:

removing said portion to form a recess in said conductive material; and

filling said recess with a material having a resistivity greater than the resistivity of said removed portion.

13. The method of claim 1, wherein said memory material is a phase change material.

14. An electrically operated memory element, comprising:

a programmable resistance memory material; and

a conductive layer in electrical communication with said memory material, said conductive layer having a raised portion extending from an edge of said layer to a distal end adjacent said memory material.

15. The memory element of claim 14, wherein conductive layer is a conductive sidewall layer.

16. The memory element of claim 14, wherein said conductive layer is a conductive liner or a conductive spacer.

17. The memory element of claim 14, wherein said memory material is a phase-change material.

18. An electrical contact for a semiconductor device,

comprising: an insulative layer;

an opening formed in said insulative layer, said opening having a sidewall surface and a bottom surface; and

a conductive layer disposed on said sidewall surface of said opening, said layer having a raised portion extending from an edge of said conductive layer on said sidewall surface.

19. The memory element of claim 18, wherein said memory material is a phase-change material.

20. A method for making a programmable resistance memory element, comprising:

providing a conductive material;

forming a sidewall spacer over a portion of said conductive material;

removing a portion of said conductive material to form a raised portion extending from said conductive material under said spacer; and

forming a programmable resistance material adjacent to at least a portion of said raised portion.

21. The method of claim 20, wherein said forming said sidewall spacer step comprises:

forming a first layer over said conductive material;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

22. The method of claim 21, wherein said forming said sidewall surface step, comprises:

forming a forth layer over said second layer;

removing a portion of said forth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

23. The method of claim 21, wherein said first and third layers are oxides and said second layer is polysilicon.

24. The method of claim 21, wherein said first and third layers are nitrides and said second layer is an oxide.

25. The method of claim 21, wherein said sidewall spacer comprises a material selected from the group consisting of dielectric, conductor and semiconductor.

26. The method of claim 20, wherein said sidewall spacer comprises a material selected from the group consisting of oxide and nitride.

27. The method of claim 20, wherein said sidewall spacer

comprises polysilicon.

28. The method of claim 20, wherein said programmable resistance material comprises a phase change material.

29. A method for making a programmable resistance memory element, comprising:

providing a conductive layer;

forming a raised portion extending from an edge of said conductive layer; and

forming a programmable resistance material adjacent to at a least a portion of said raised portion.

30. The method of claim 29, wherein said forming said raised portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said raised portion under said mask.

31. The method of claim 30, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

32. The method of claim 31, wherein said forming said sidewall spacer step comprises:

forming a first layer over said edge;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

33. The method of claim 32, wherein said first and third layers are oxides and said second layer is polysilicon.

34. The method of claim 32, wherein said first and third layers are nitrides and said second layer is an oxide.

35. The method of claim 29, wherein said programmable resistance material comprises a phase change material.

36. A method of forming a programmable resistance memory element, comprising:

providing a first dielectric layer;

forming a sidewall surface in said dielectric layer;

forming a conductive layer on said sidewall surface;

forming a second dielectric layer over said conductive layer;

forming or exposing an edge of said conductive layer;

forming a raised portion extending from said edge of said conductive layer; and

forming a programmable resistance material adjacent to at least a portion of said raised portion.

37. The method of claim 36, wherein said forming said raised portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said raised portion under said mask.

38. The method of claim 37, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

39. The method of claim 38, wherein said forming said sidewall spacer step comprises:

forming a first layer over said edge;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

40. The method of claim 39, wherein said first and third layers are oxides and said second layer is polysilicon.

41. The method of claim 39, wherein said first and third layers are nitrides and said second layer is an oxide.

42. The method of claim 36, wherein said programmable resistance material comprises a phase change material.

43. A method for making an electrode for a semiconductor device, comprising:

providing a conductive layer; and

forming a raised portion extending from an edge of said conductive layer.

44. The method of claim 43 herein said forming said raised portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said raised portion under said mask.

45. The method of claim 44, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

46. The method of claim 45, wherein said forming said sidewall spacer step comprises:

forming a first layer over said edge;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

47. The method of claim 46, wherein said first and third layers are oxides and said second layer is polysilicon.

48 The method of claim 46, wherein said first and third layers
are nitrides and said second layer is an oxide.

49. A method of making an electrode for a semiconductor device, comprising:

providing a first dielectric layer;

forming a sidewall surface in said dielectric layer;

forming a conductive layer on said sidewall surface;

forming a second dielectric layer over said conductive layer;

forming or exposing an edge of said conductive layer; and

forming a raised portion extending from said edge of said conductive layer.

50. The method of claim 49, wherein said forming said raised portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said raised portion under said mask.

51. The method of claim 50, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

52. The method of claim 51, wherein said forming said sidewall spacer step comprises:

forming a first layer over said edge;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

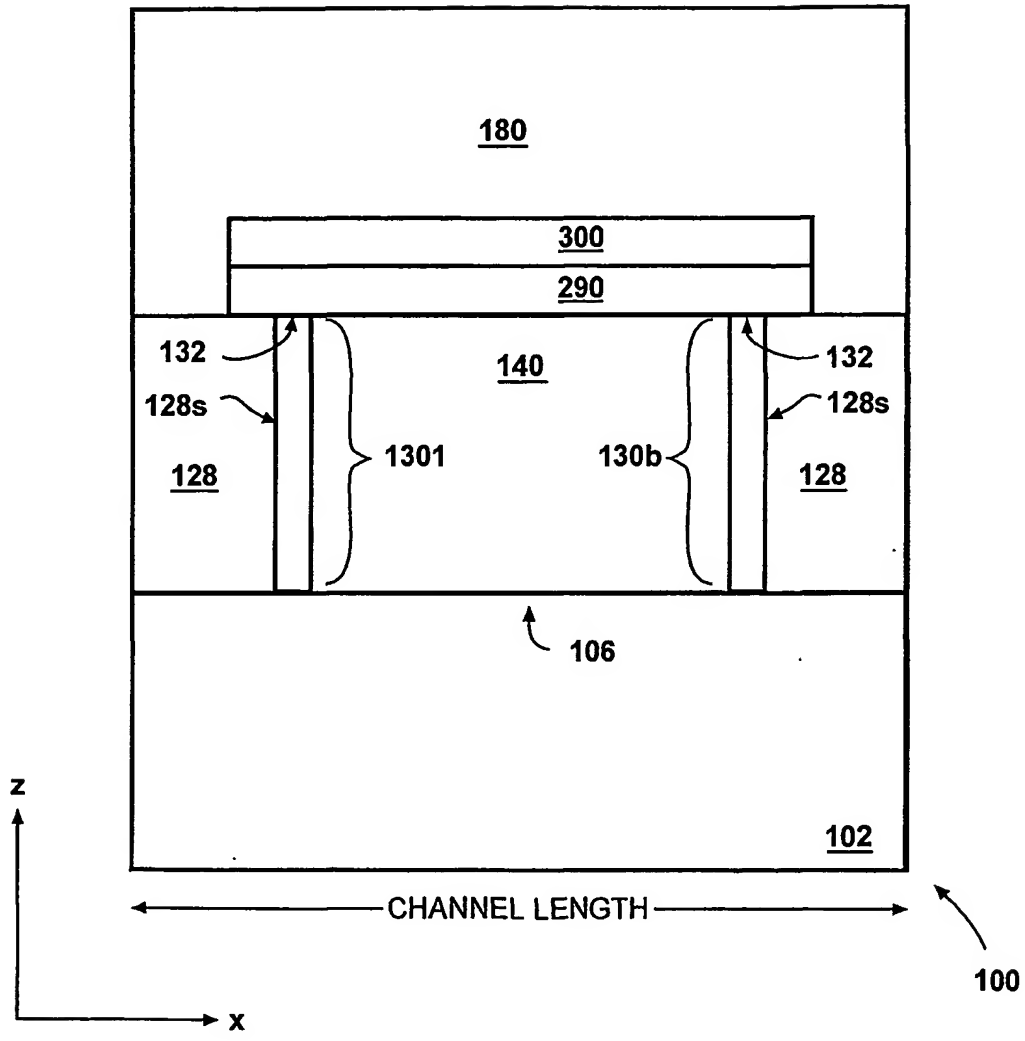
removing said second layer; and

removing a portion of said first layer.

53. The method of claim 52, wherein said first and third layers are oxides and said second layer is polysilicon.

54. The method of claim 52, wherein said first and third layers are nitrides and said second layer is an oxide.

FIG - 1A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CHANNEL LENGTH
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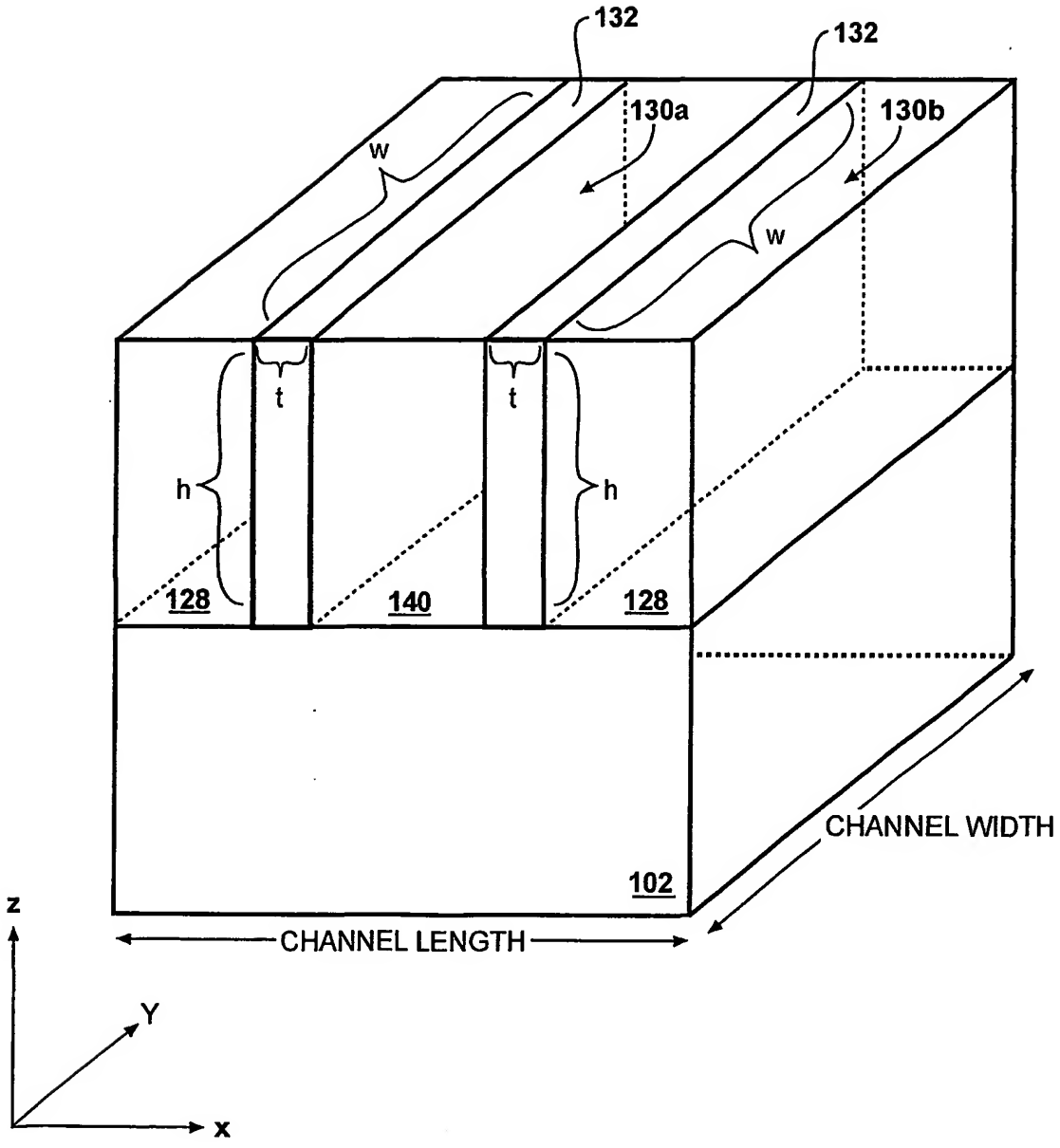
x

FIG - 1B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130a
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CHANNEL WIDTH
CHANNEL LENGTH
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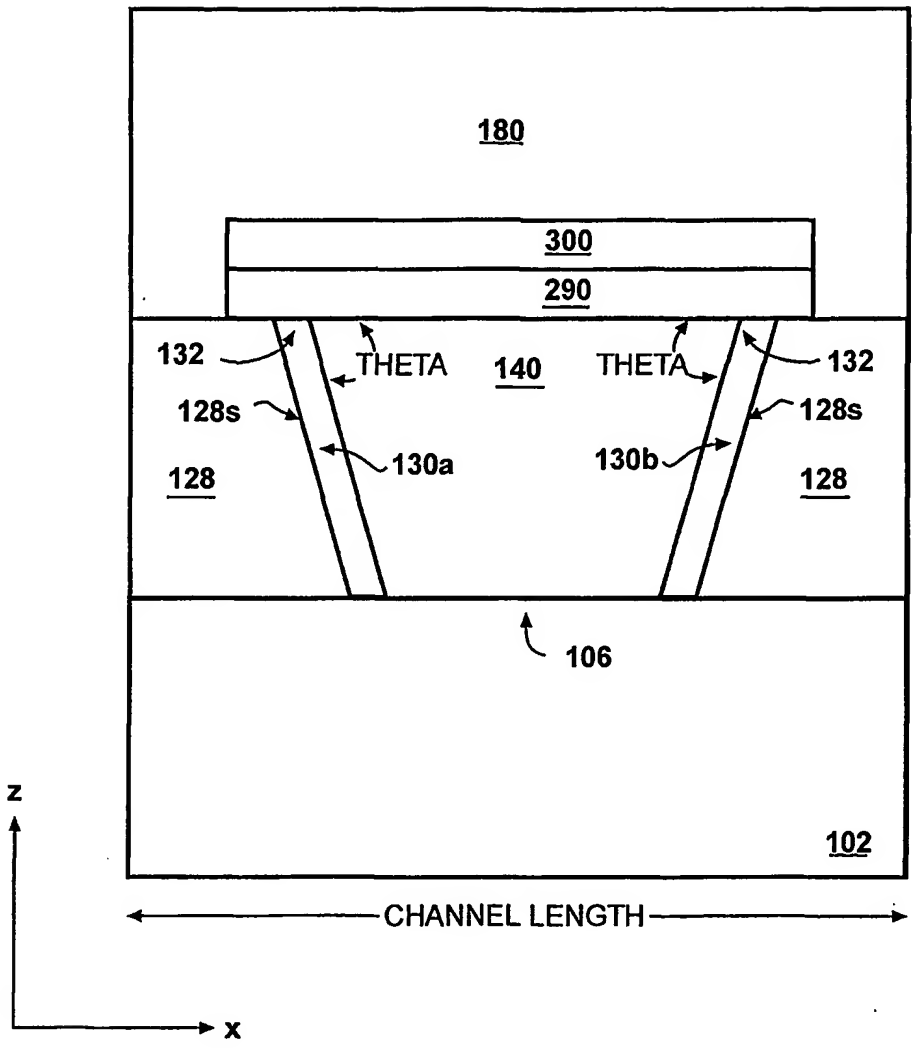
Y
x

FIG - 1C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290
132
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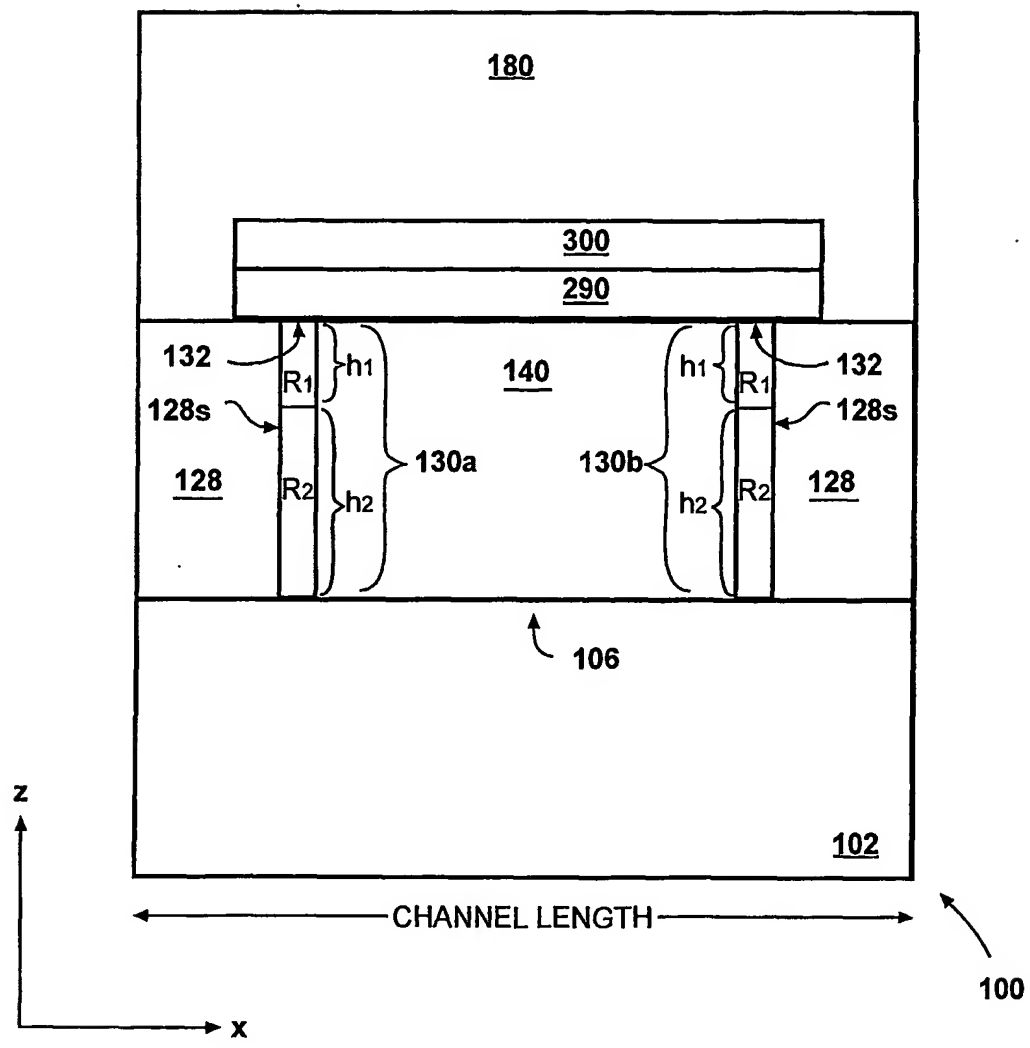
106
102
z
x
CHANNEL LENGTH

FIG - 1D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h1
140
h1
R1
132
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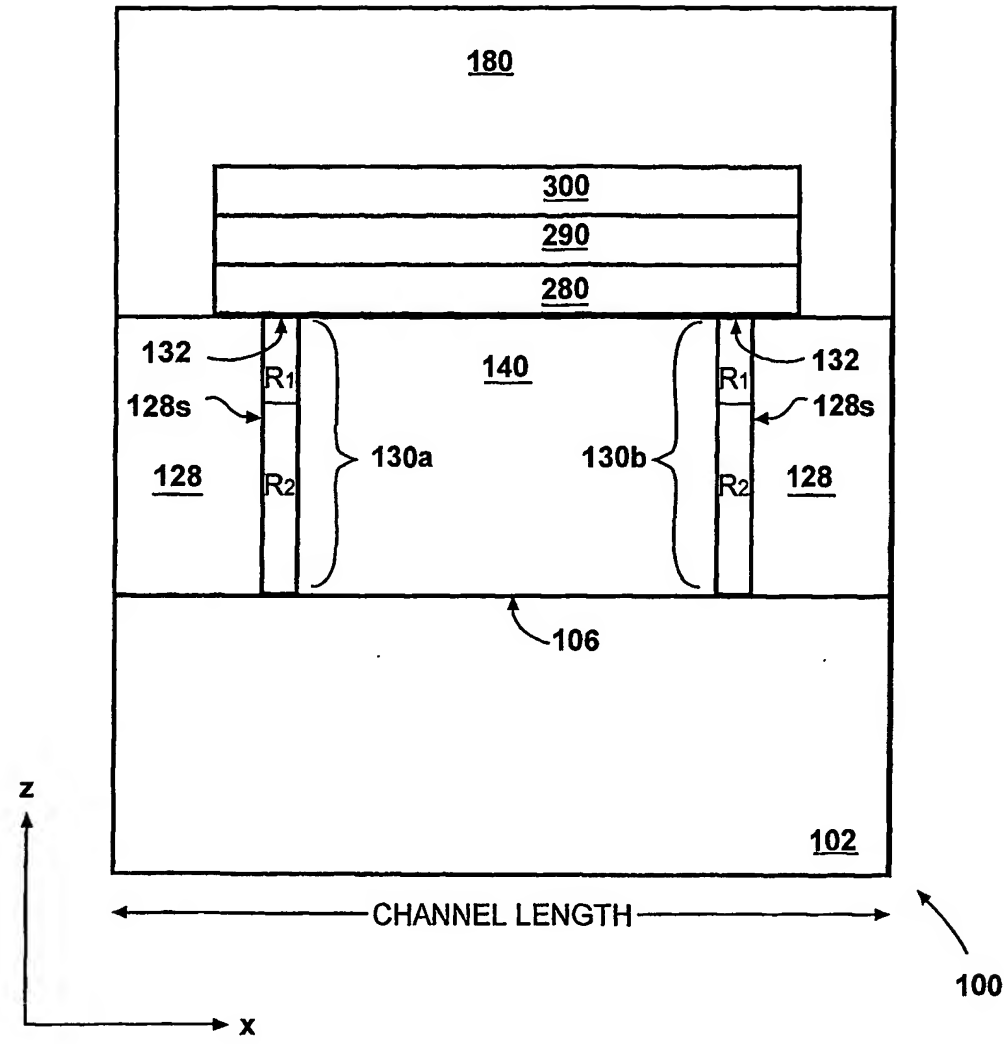
R2
128
106
102
z
CHANNEL LENGTH
100
x

FIG - 1E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300
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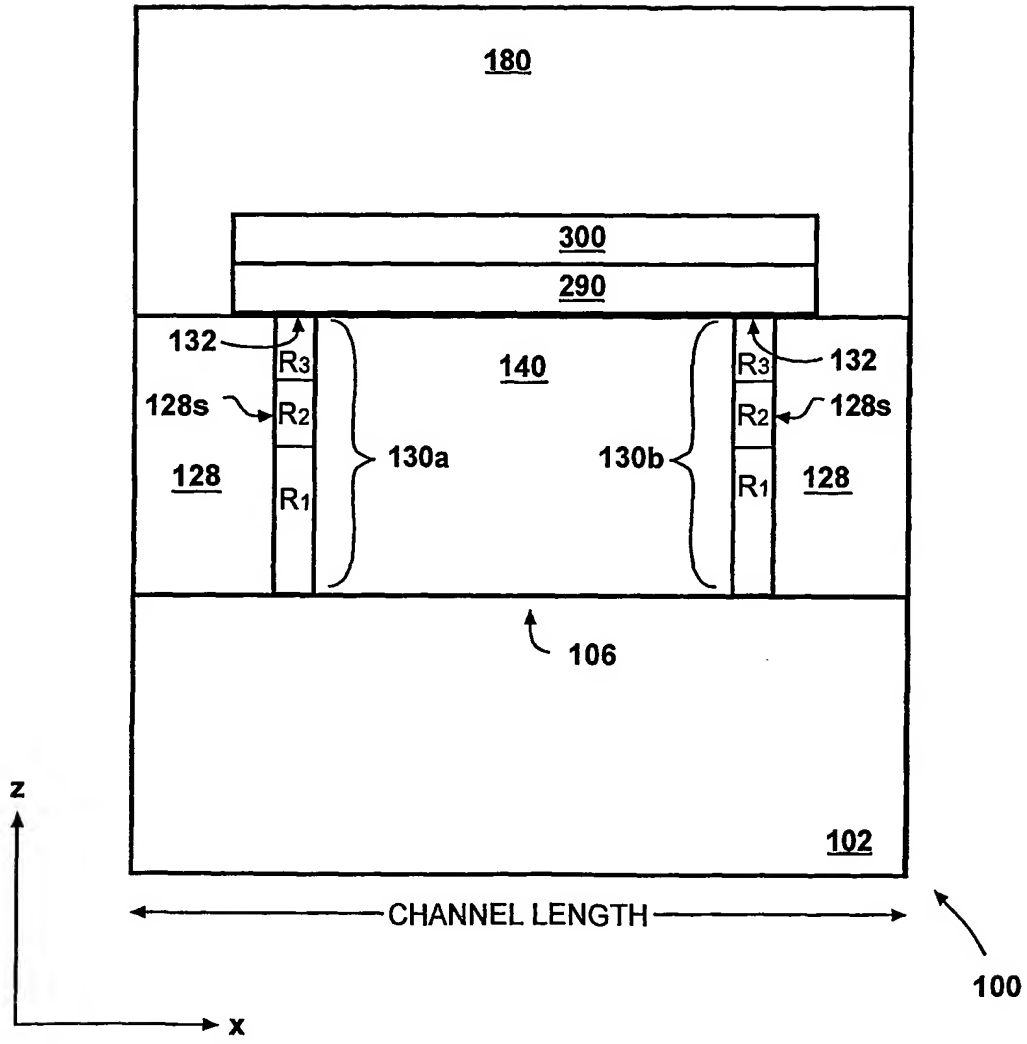
R1
R2
130a
140
130b
106
102
z
x
CHANNEL LENGTH
100

FIG - 1F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R3
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R2
128
R1
130a
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R3
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R2
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R1
128
106
102
z
x
CHANNEL LENGTH
100

FIG - 2A

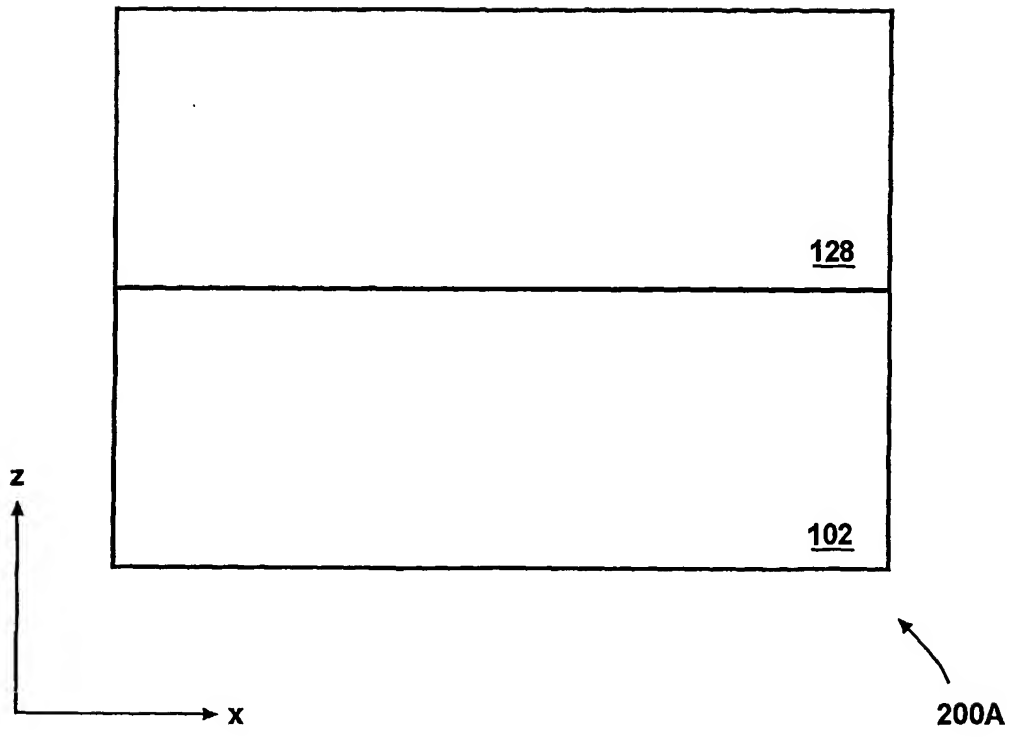


FIG - 2A'

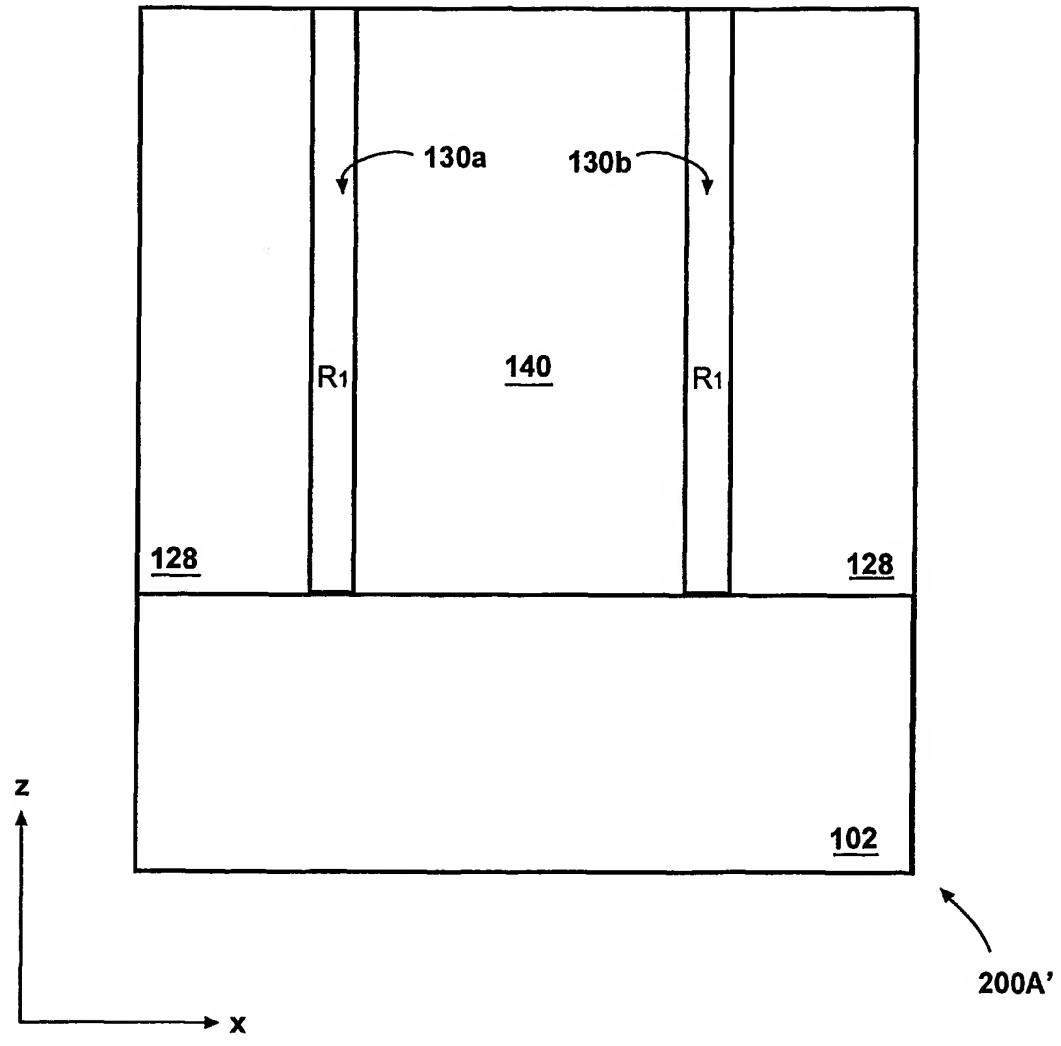


FIG - 2B

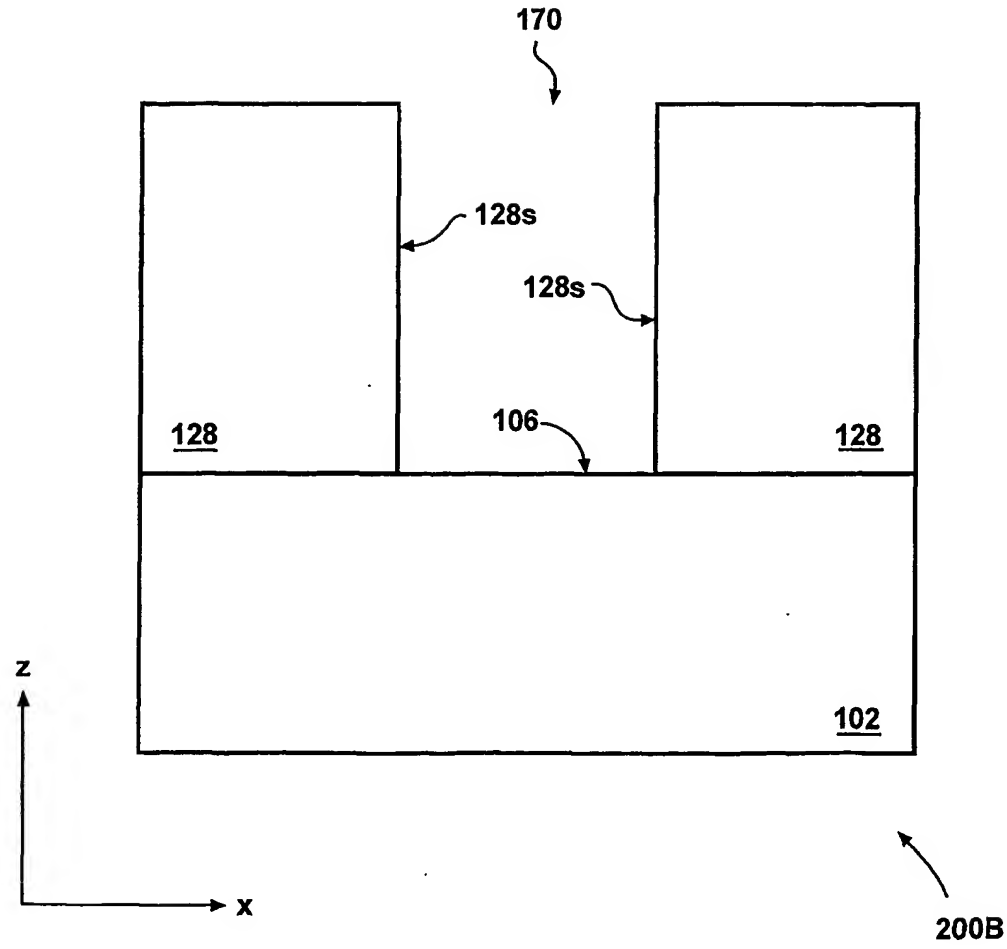


FIG - 2B'

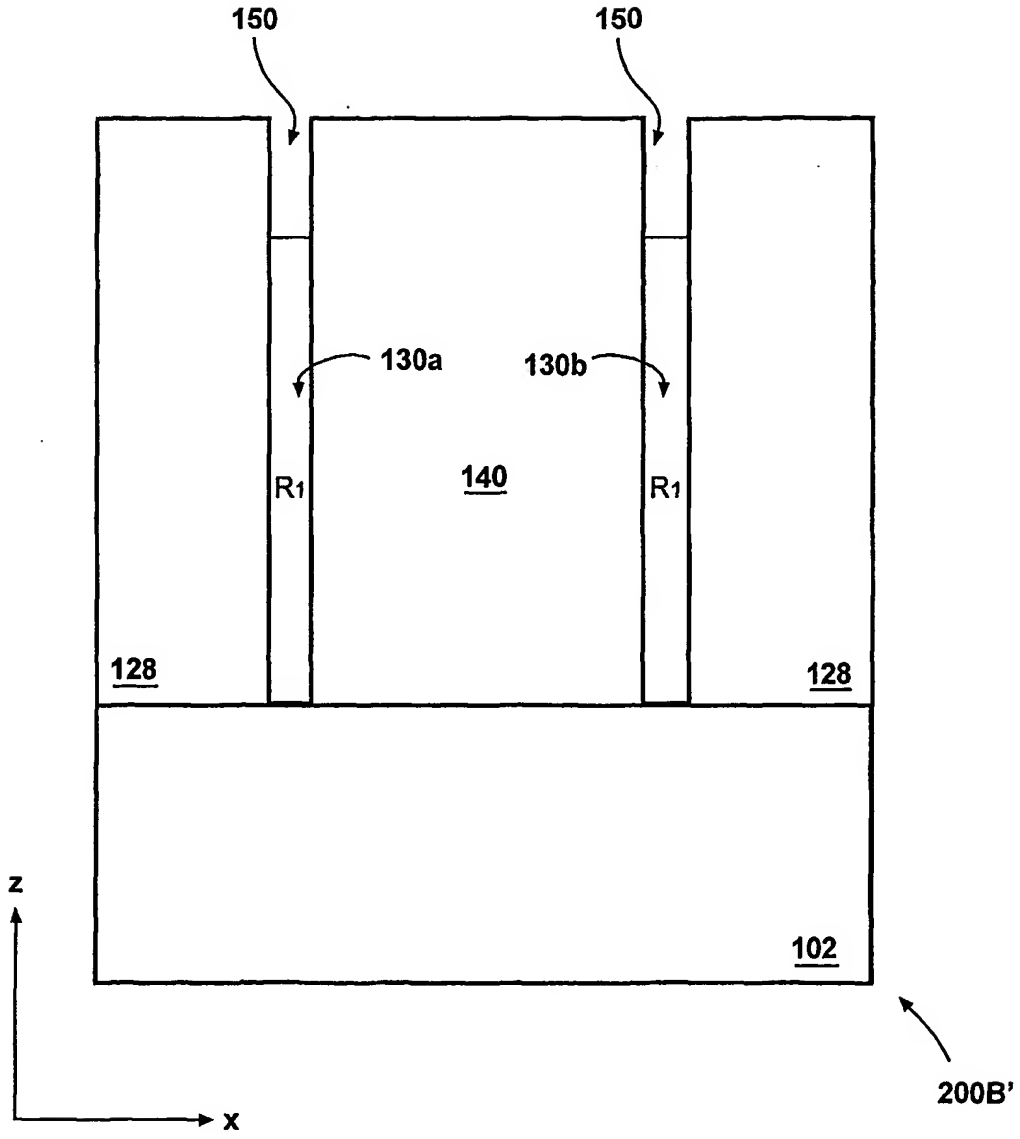
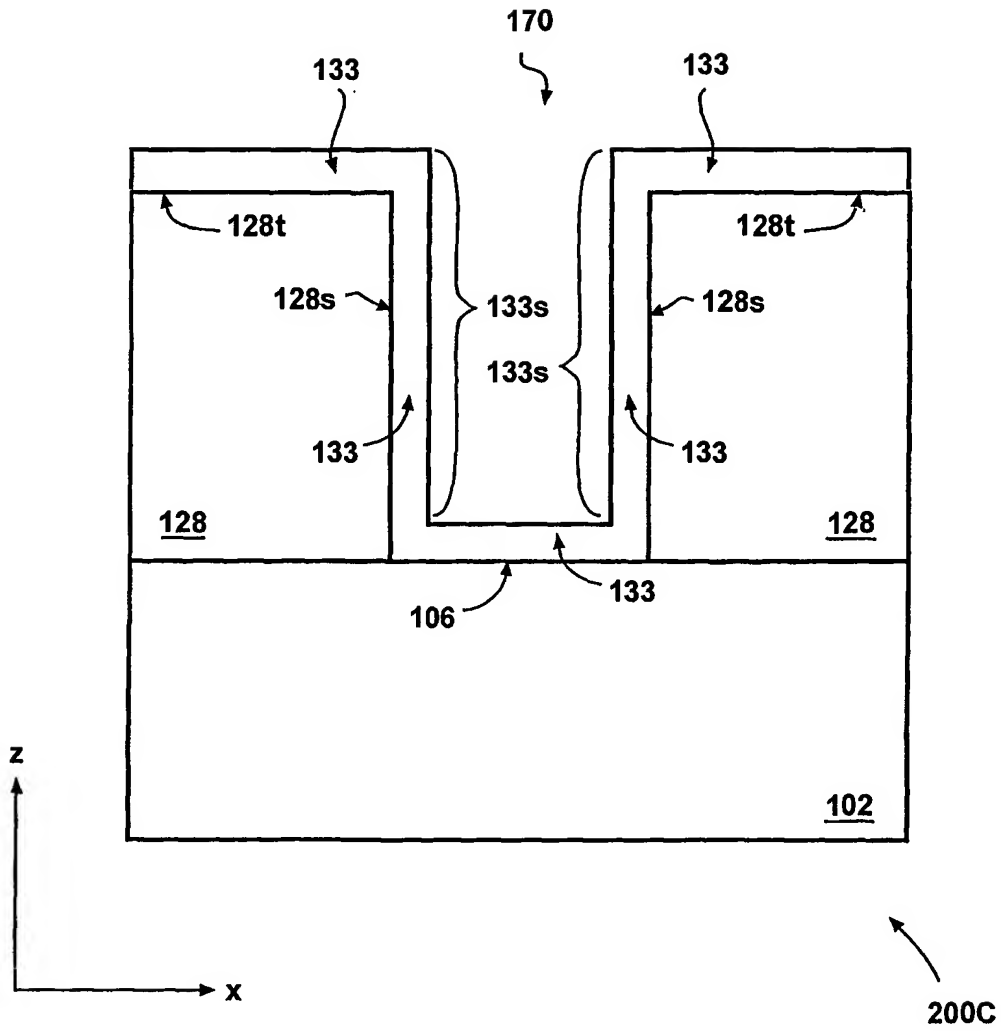


FIG - 2C


170
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133
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128t
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133
128
128
133
106
102
z
x
200C

FIG - 2C'

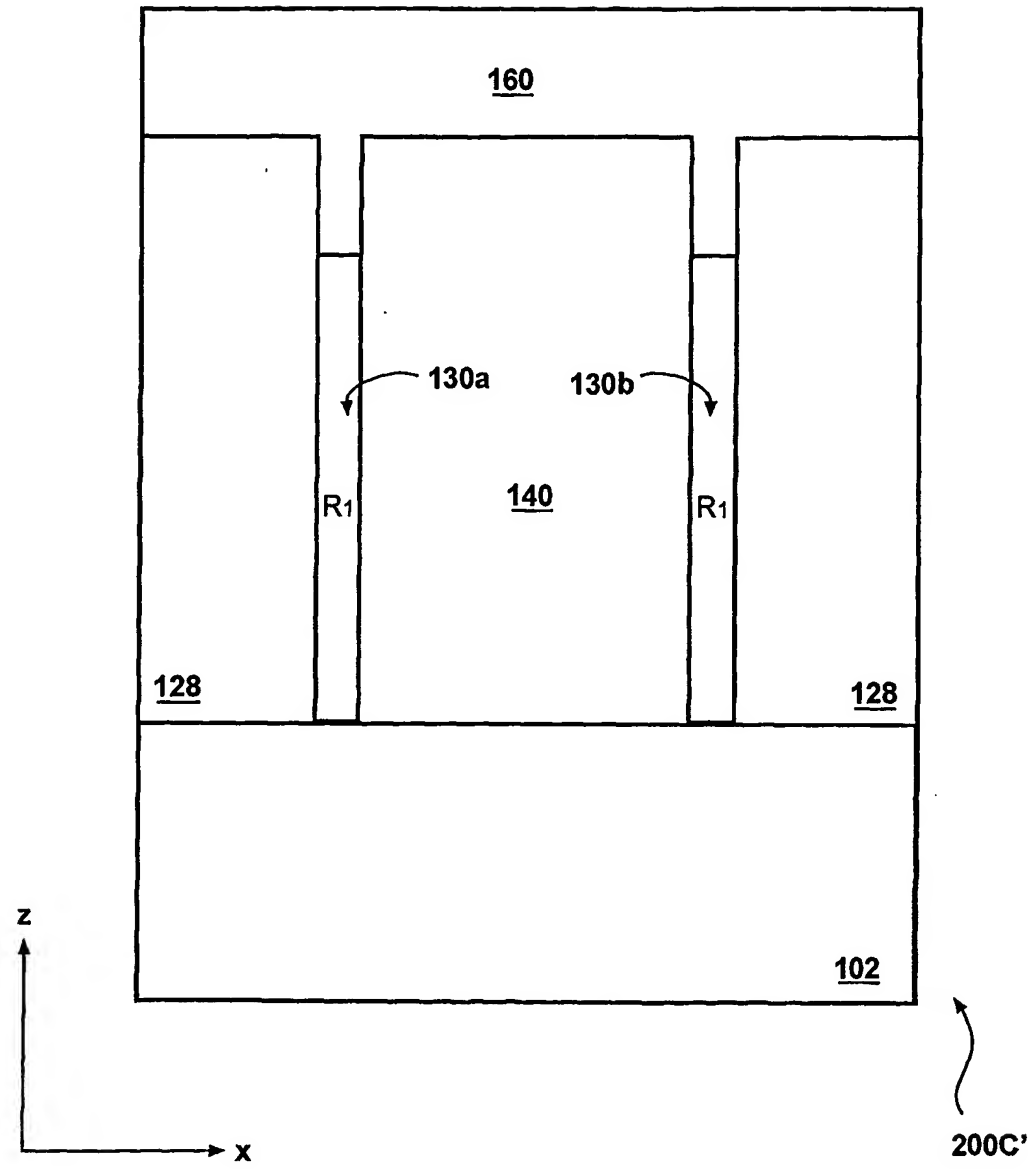


FIG - 2D

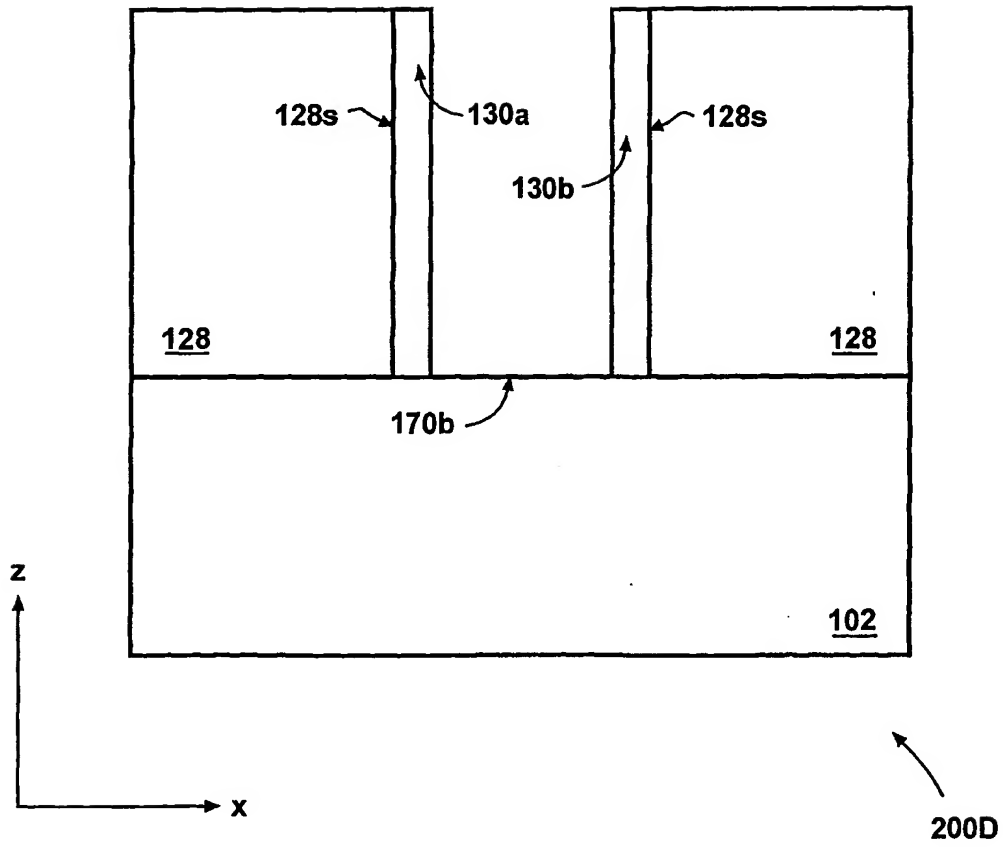


FIG - 2D'

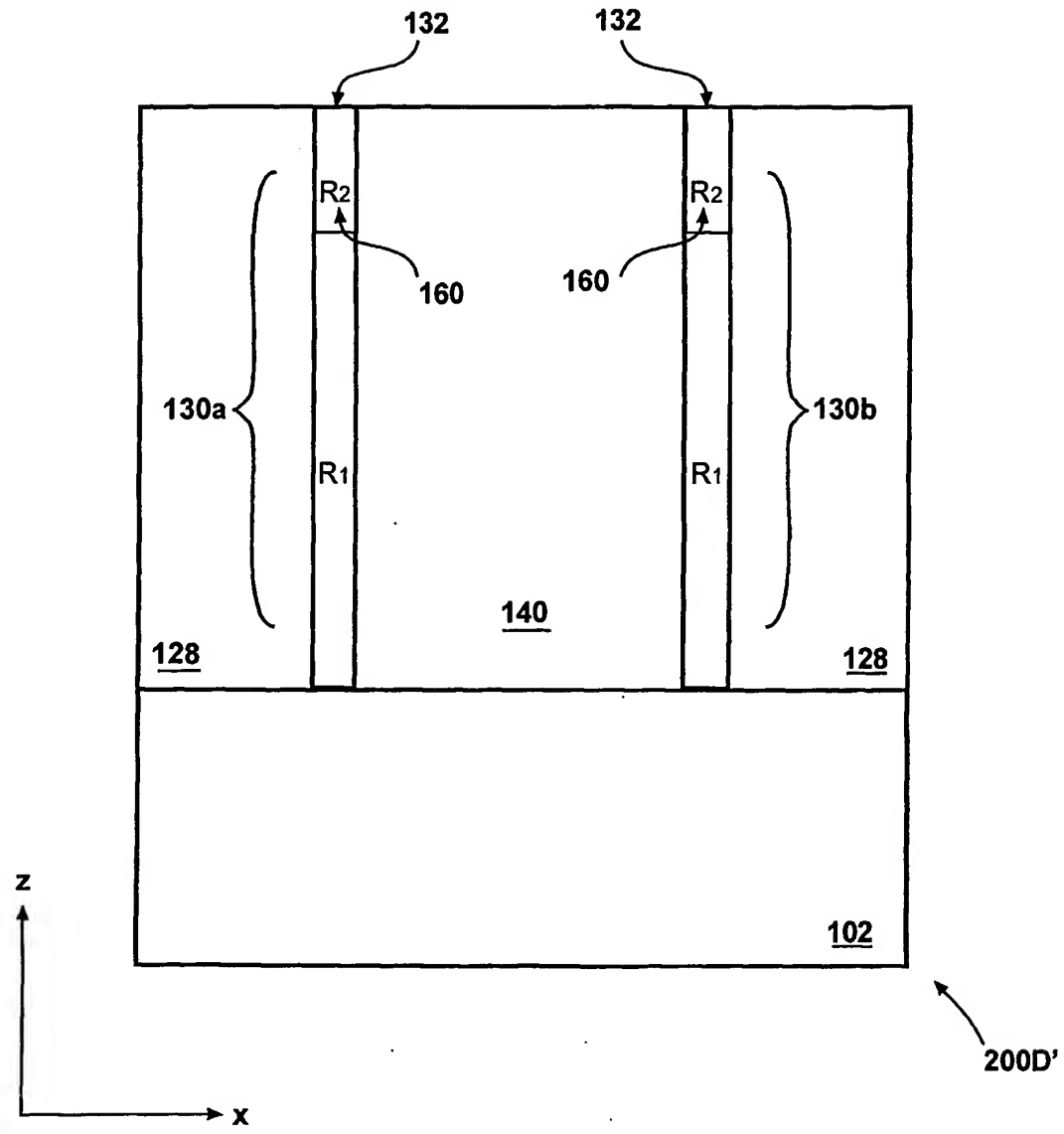


FIG - 2E

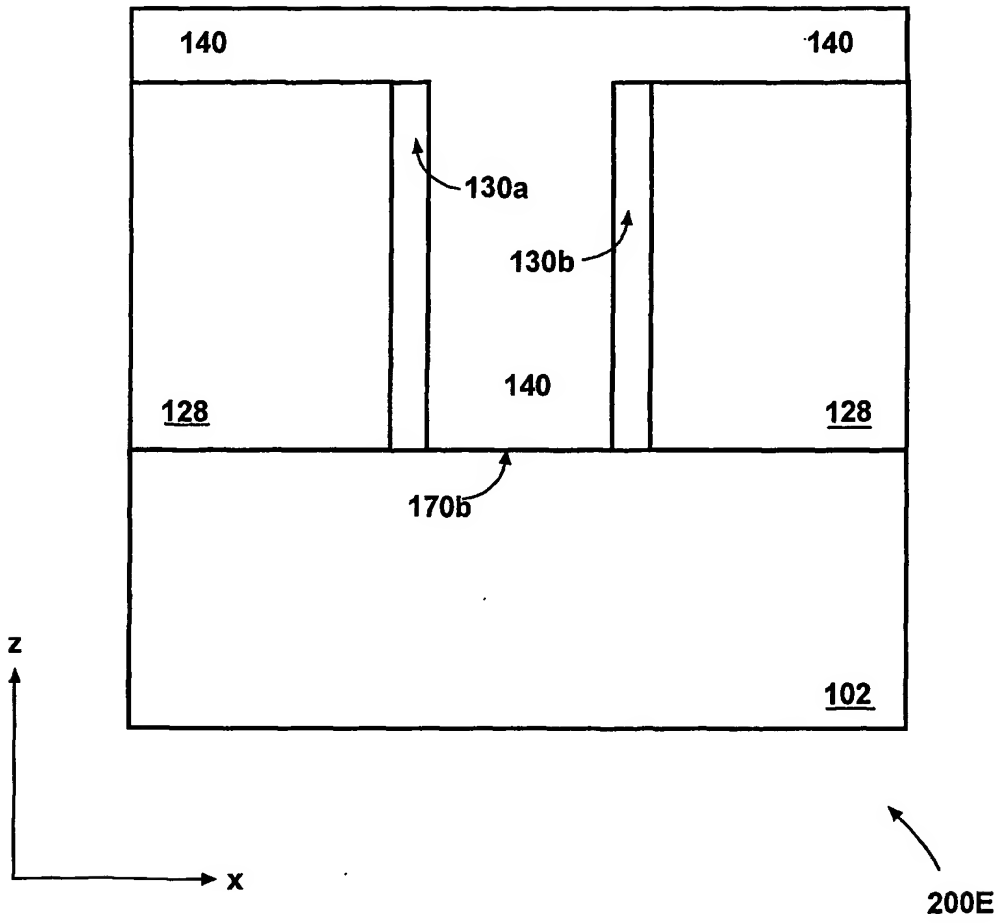


FIG - 2F

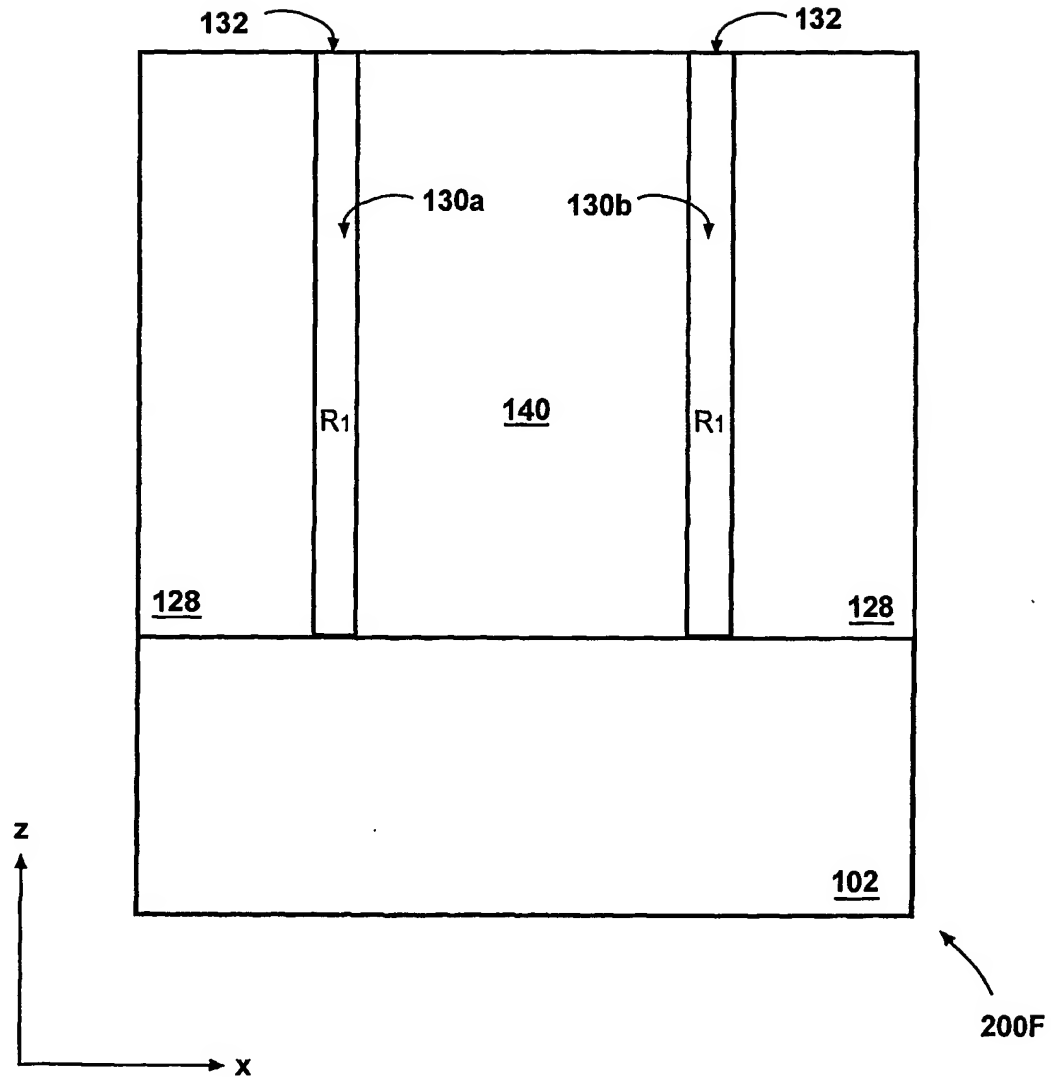


FIG - 2G

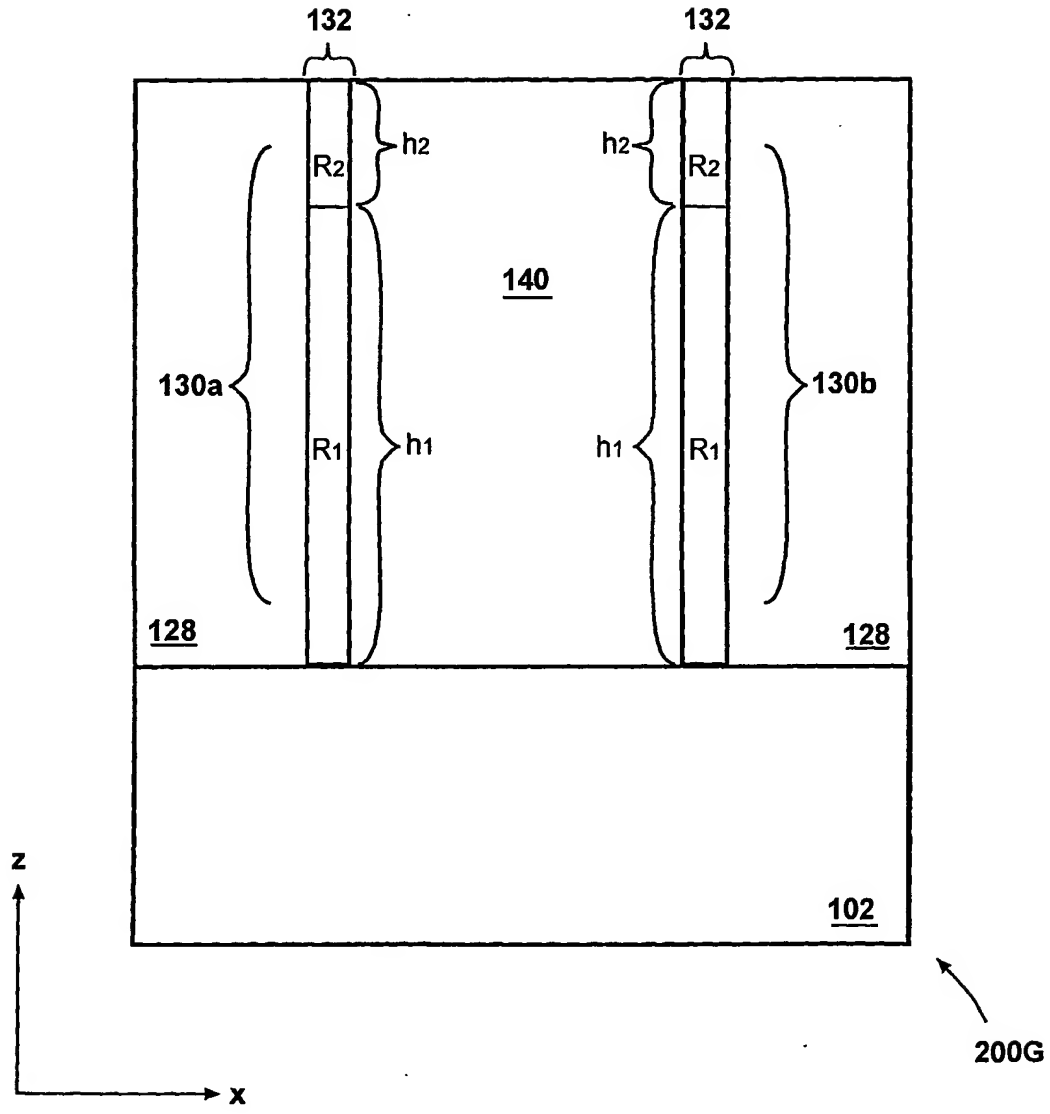


FIG - 2H

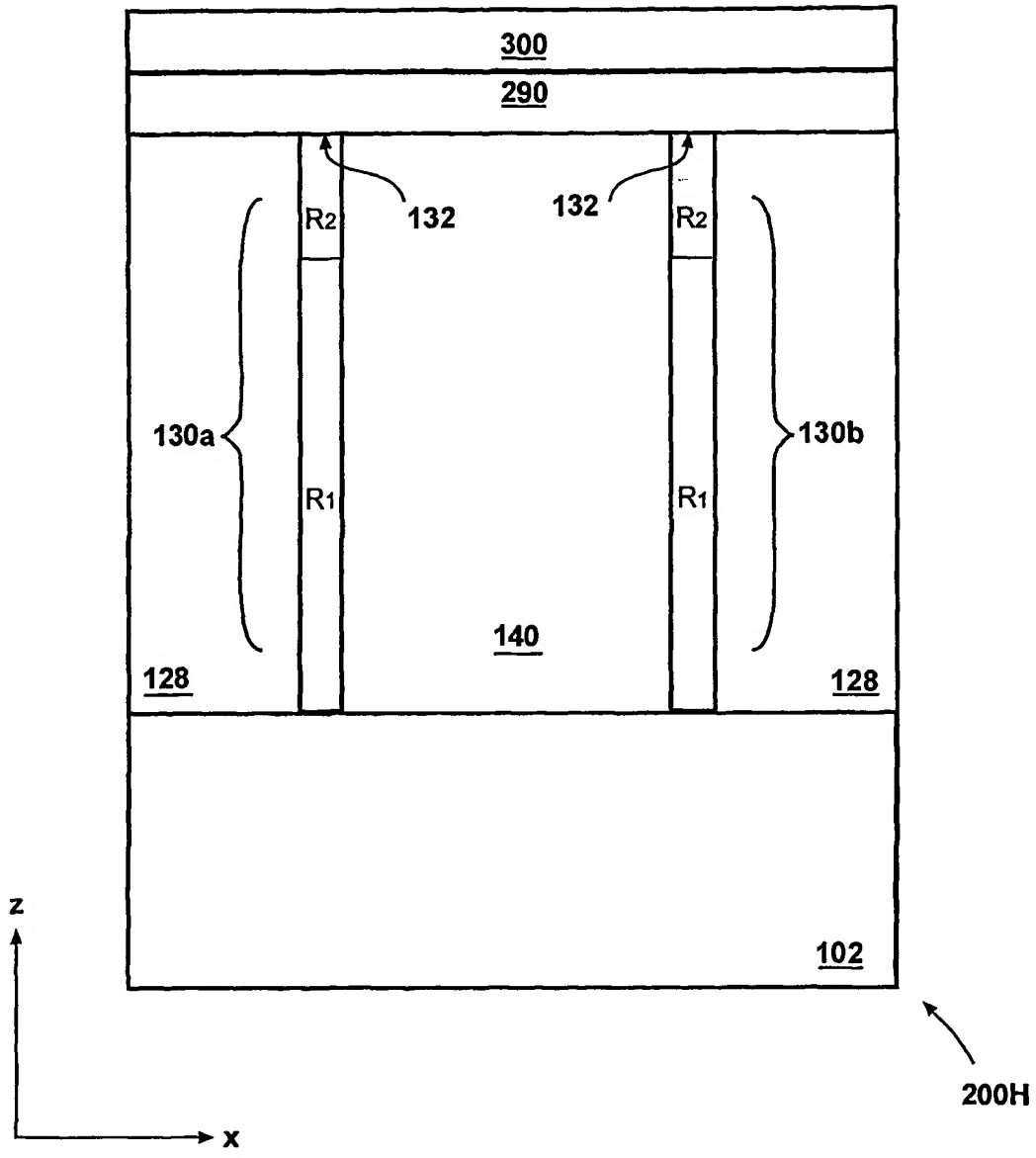


FIG - 3A

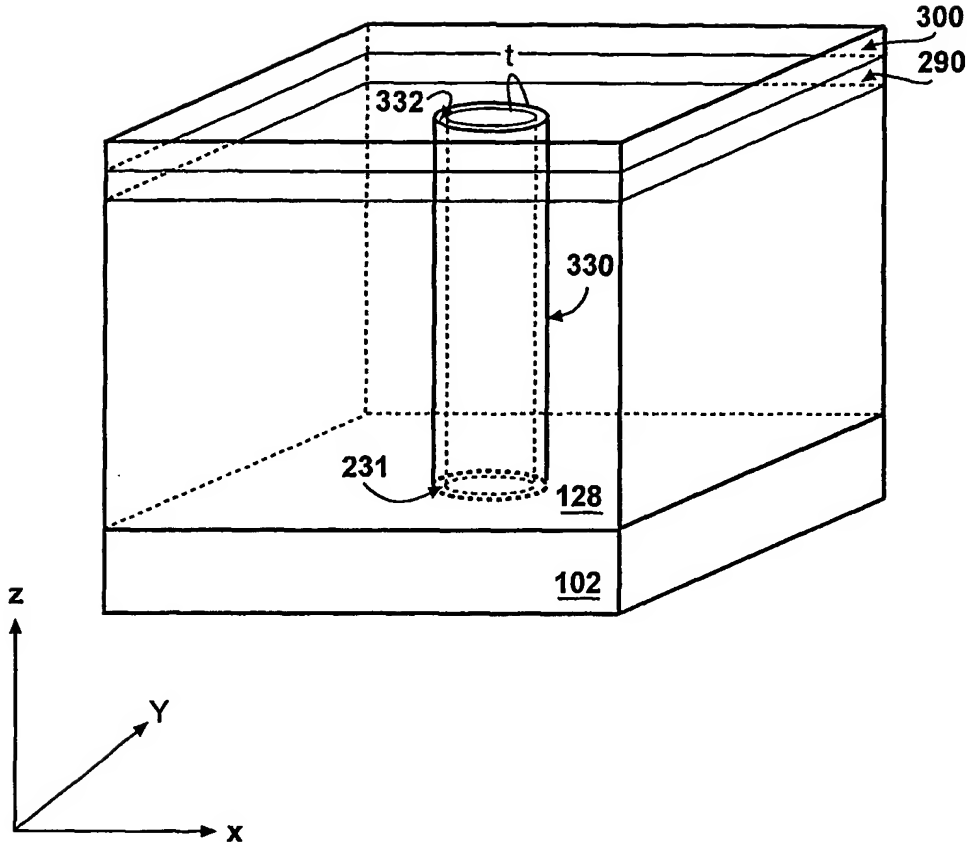


FIG - 3B

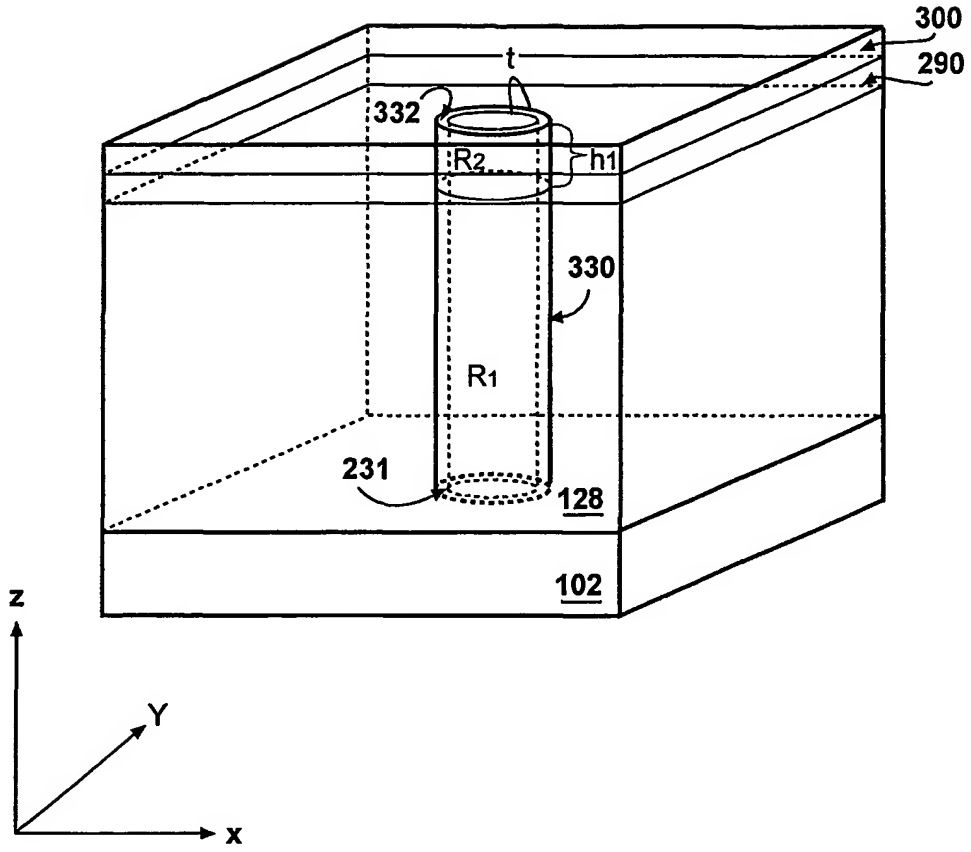


FIG - 4A

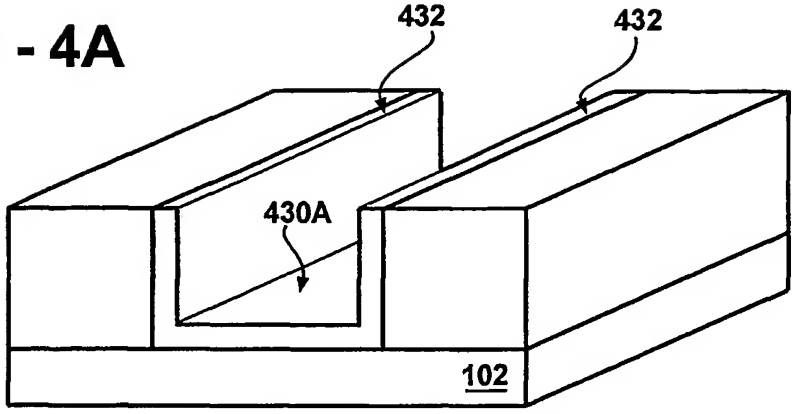


FIG - 4B

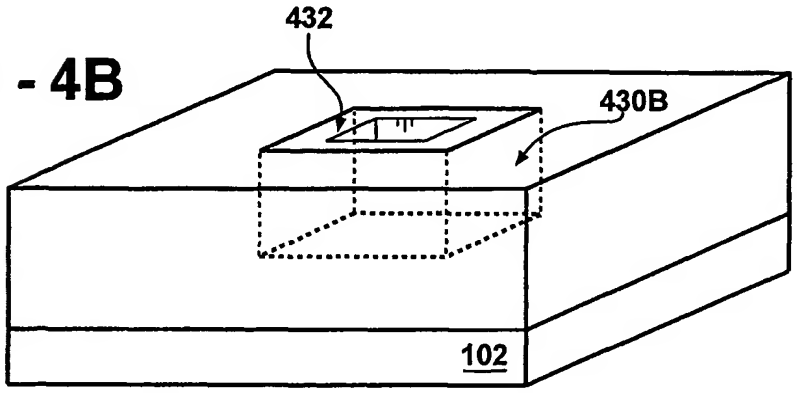


FIG - 4C

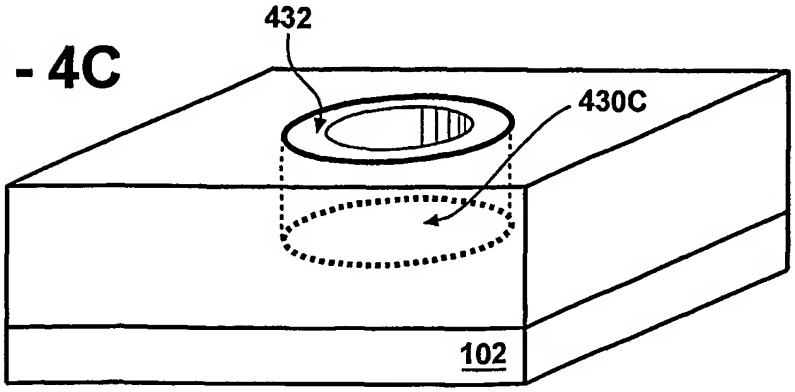


FIG - 5A

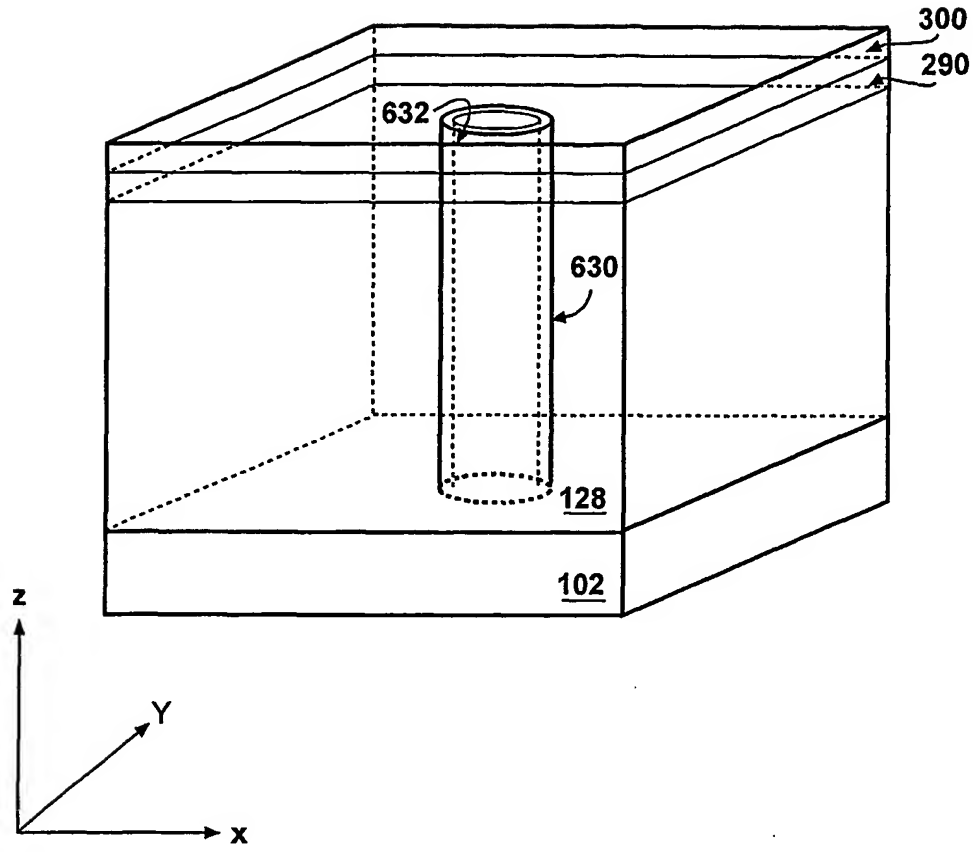


FIG - 5B

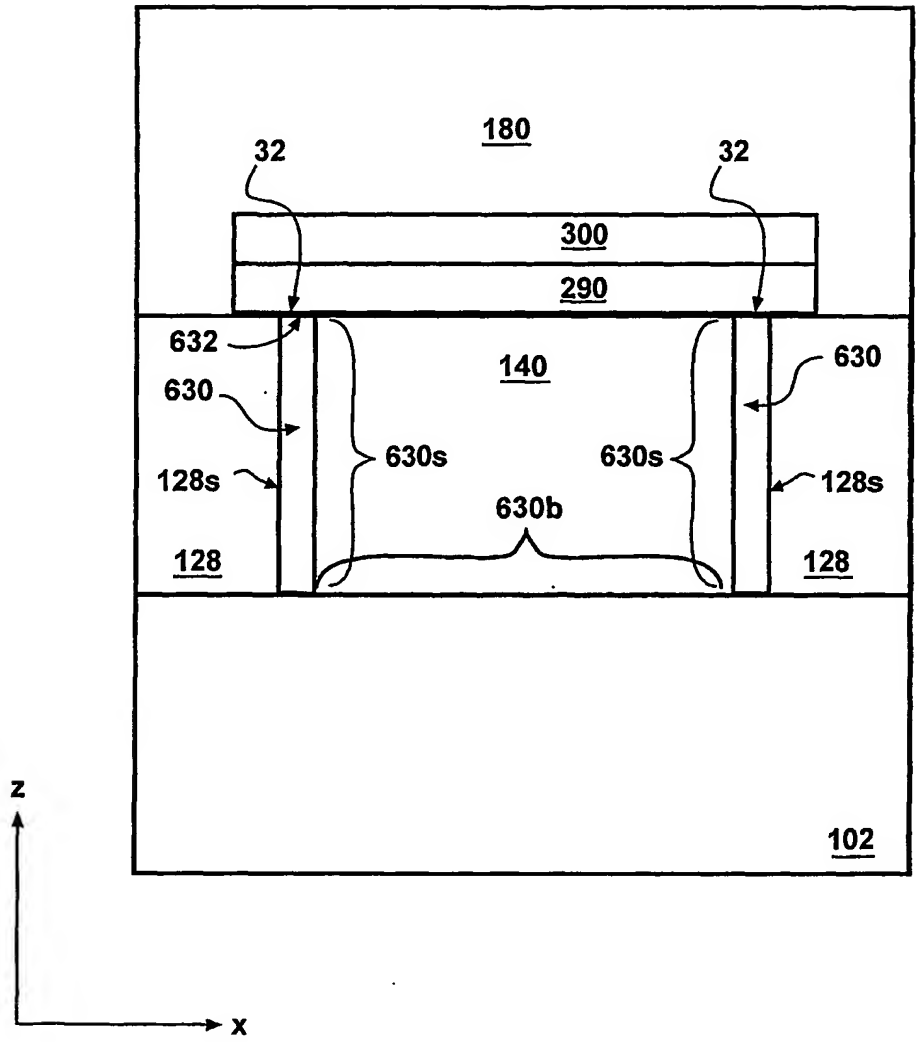
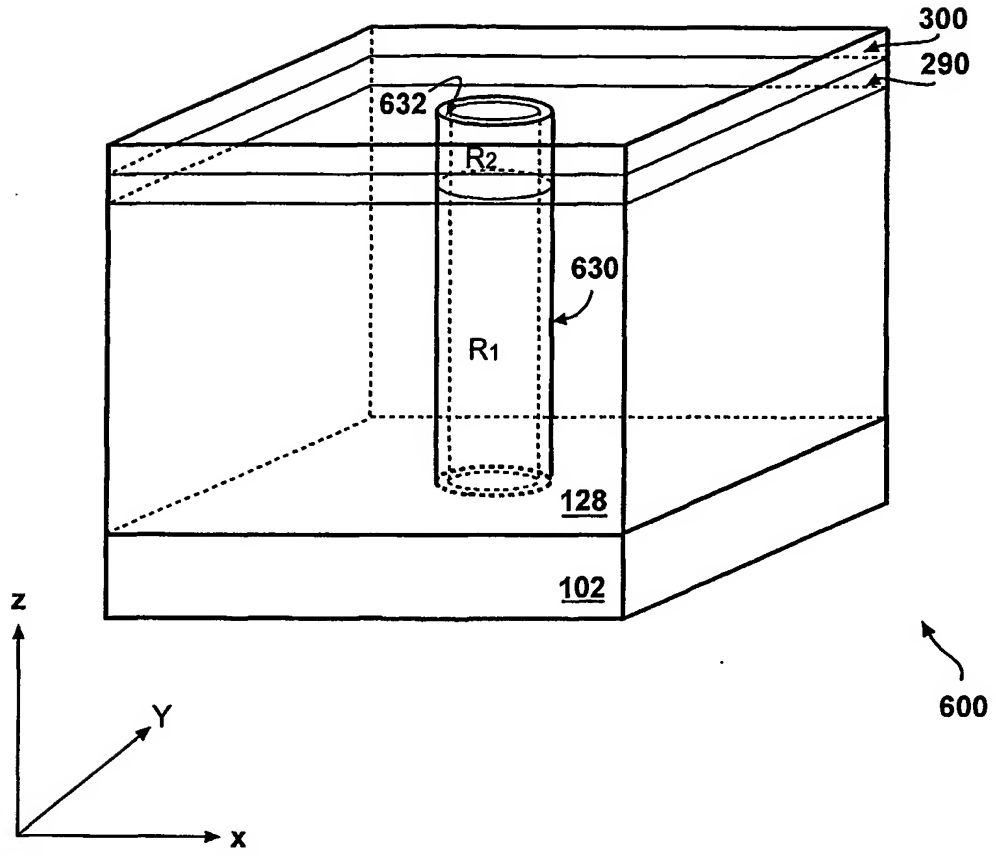

180
32
32
300
290
632
630
140
630
630s
630s
128s
128s
630b
128
128
z
x
102

FIG - 5C



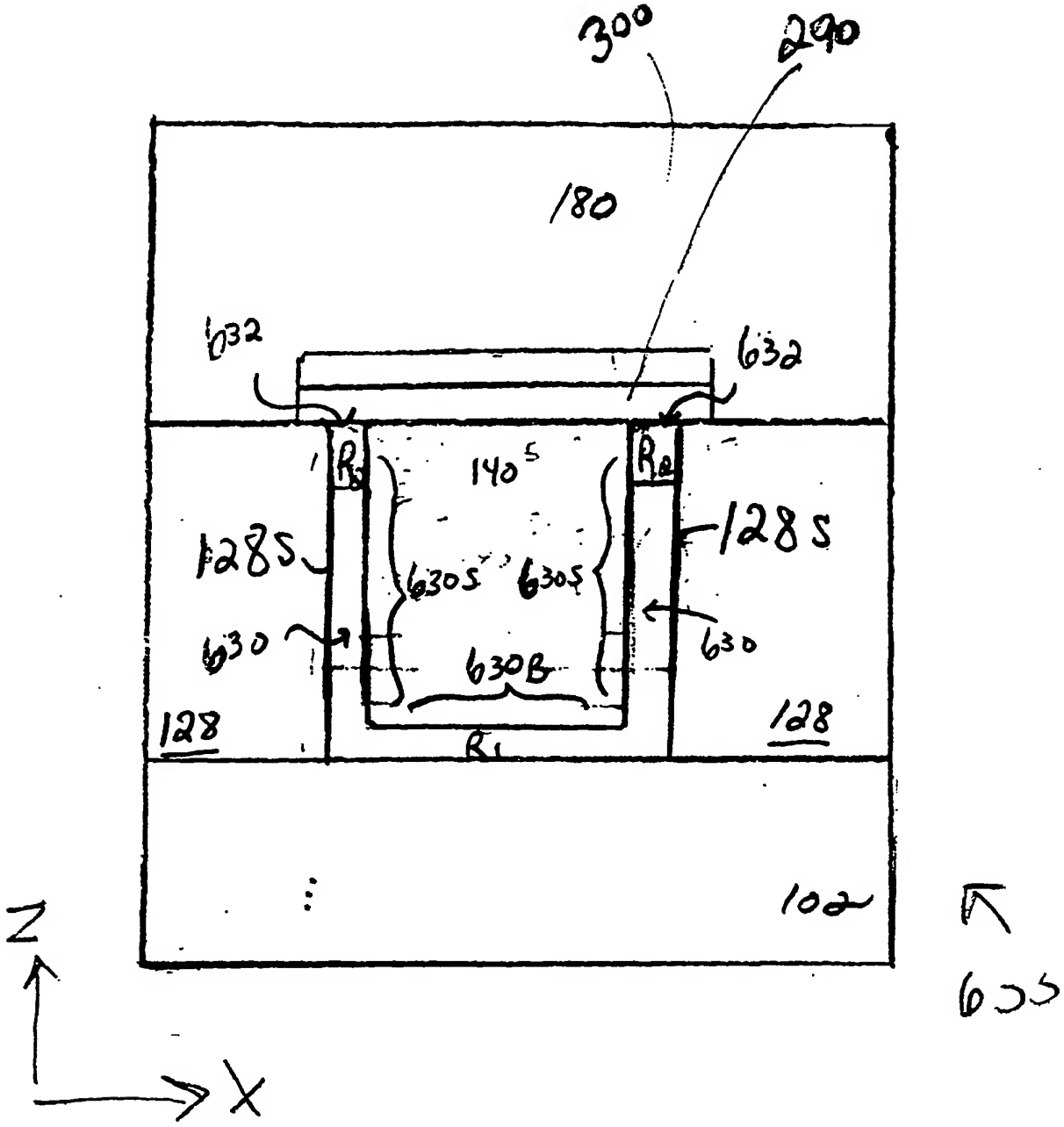

300
290
180
632
632
R_S
R_D
140
128S
128S
630S
630S
630
630
630B
128
128
R_1
102
Z
X
605

FIGURE 5D

FIG - 6A

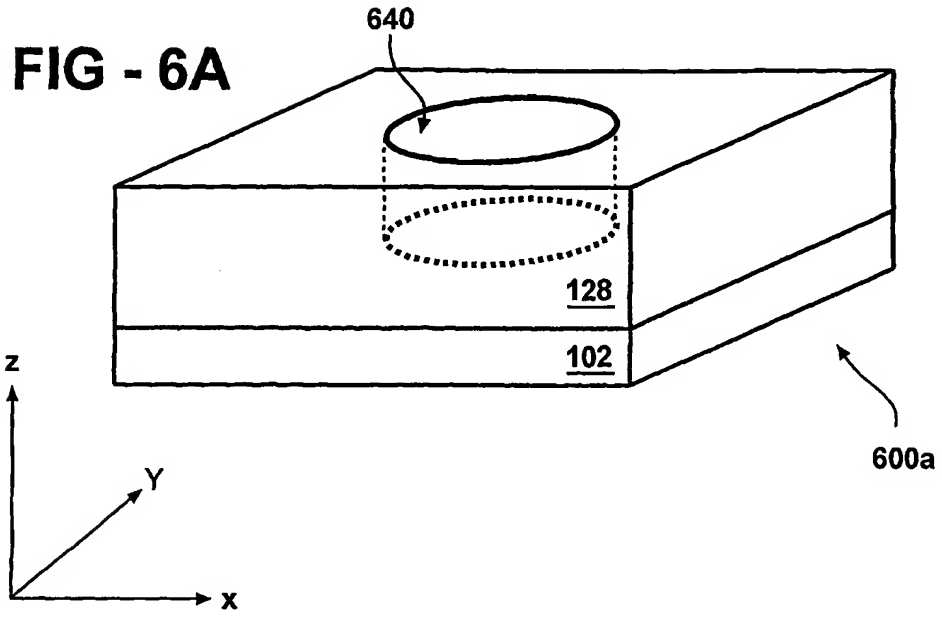


FIG - 6B

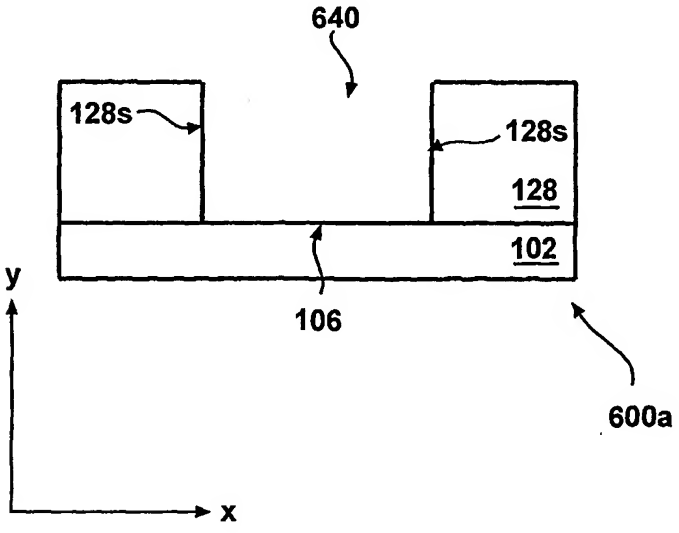


FIG - 6C

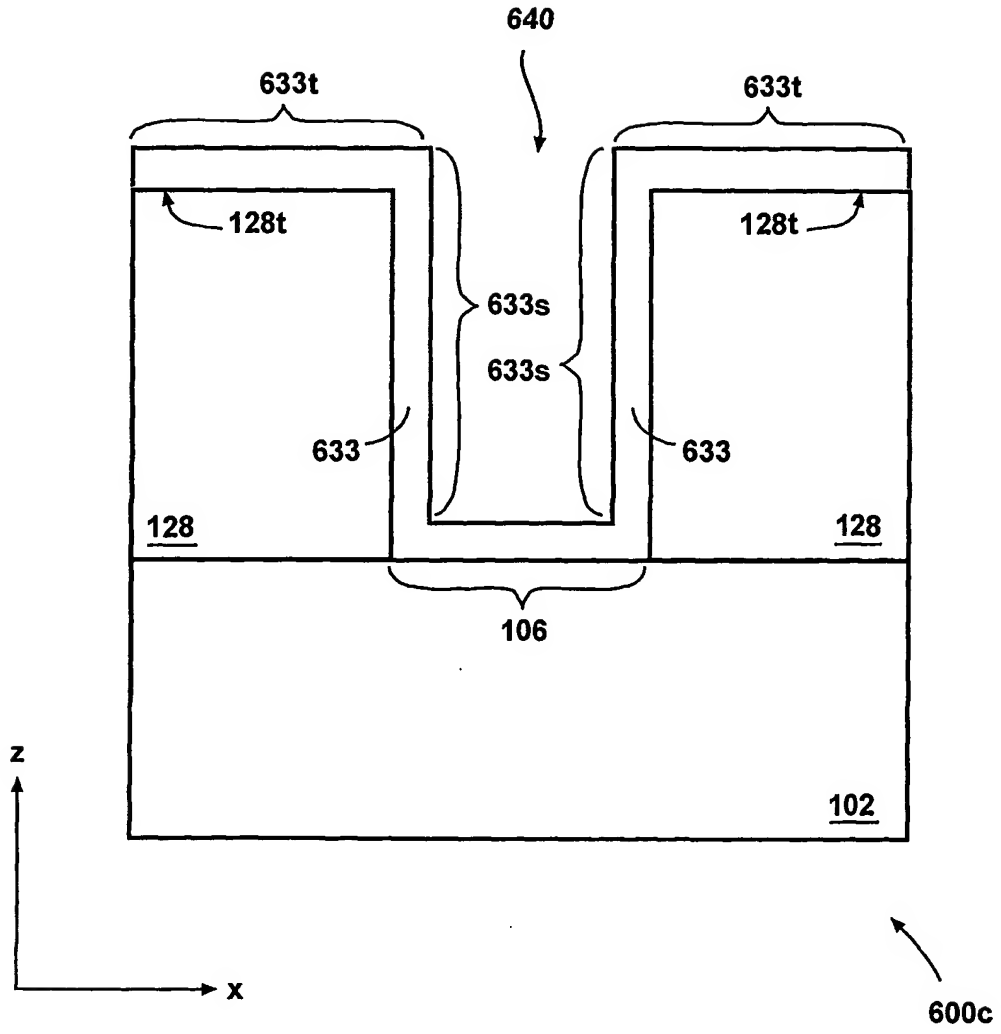

640
633t
633t
128t
128t
633s
633s
633
633
128
128
106
102
z
x
600c

FIG - 6D

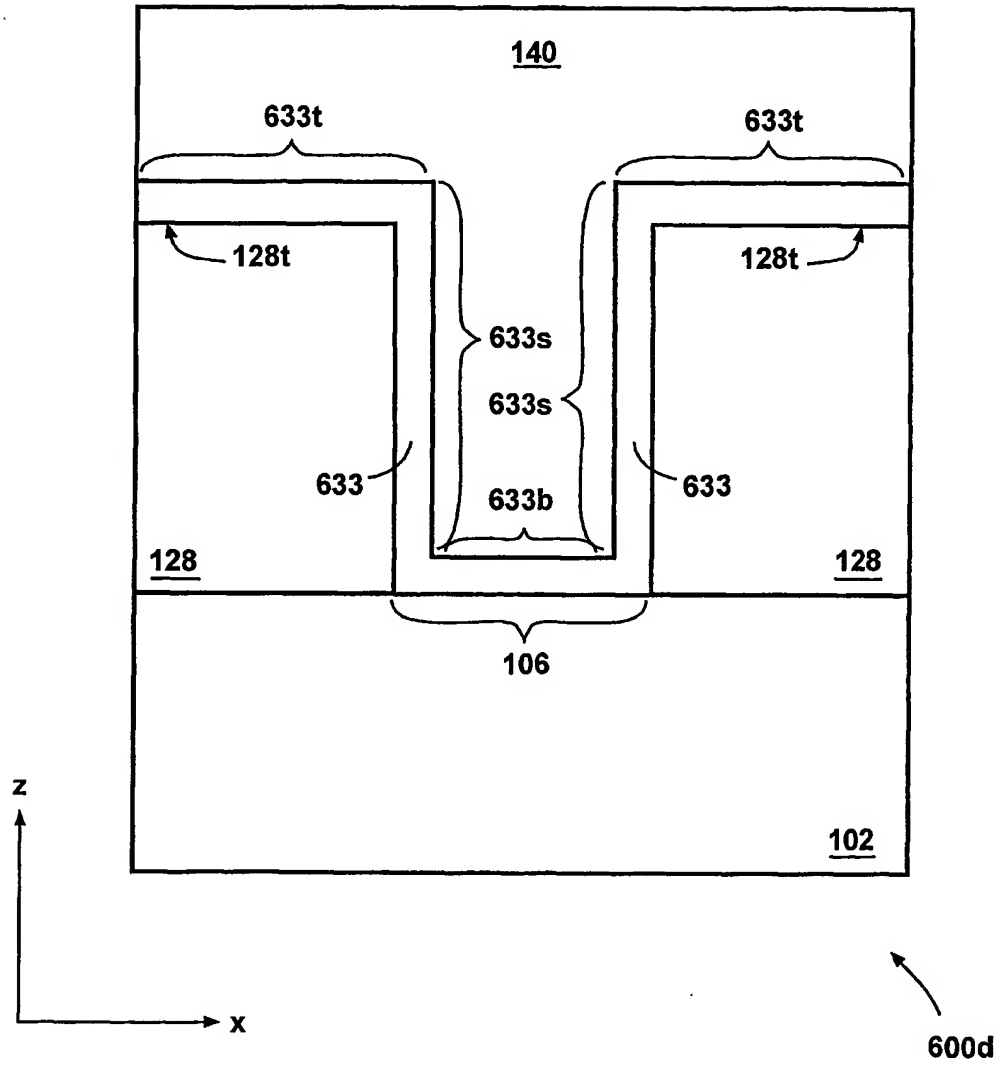

140
633t
633t
128t
128t
633s
633s
633
633b
633
128
128
106
102
z
x
600d

FIG - 6E

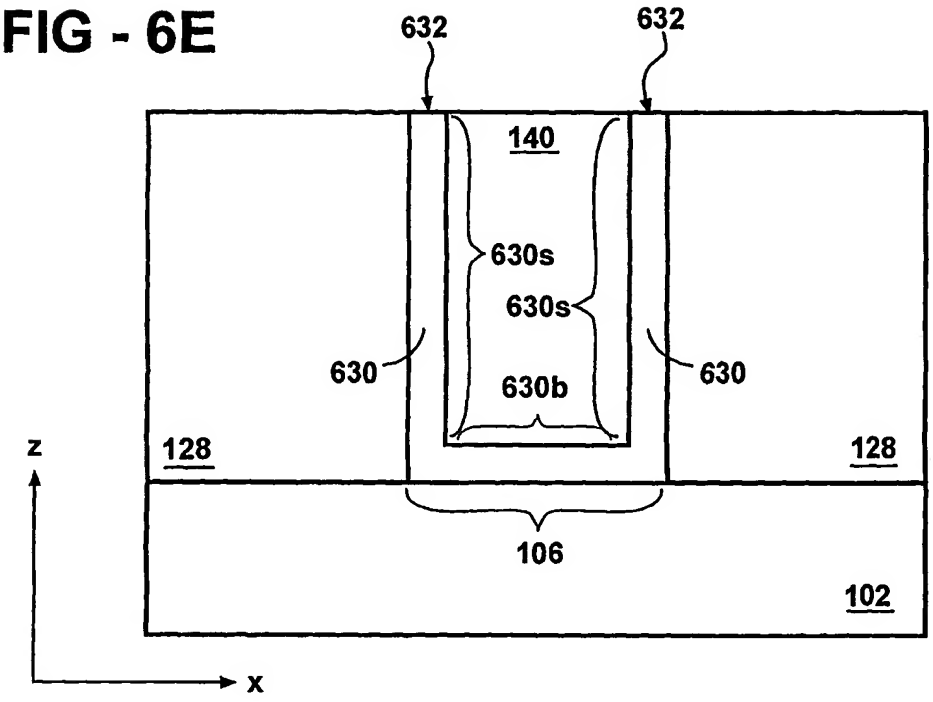

632
632
140
630s
630s
630
630b
630
128
128
106
102
z
x

FIG - 6F

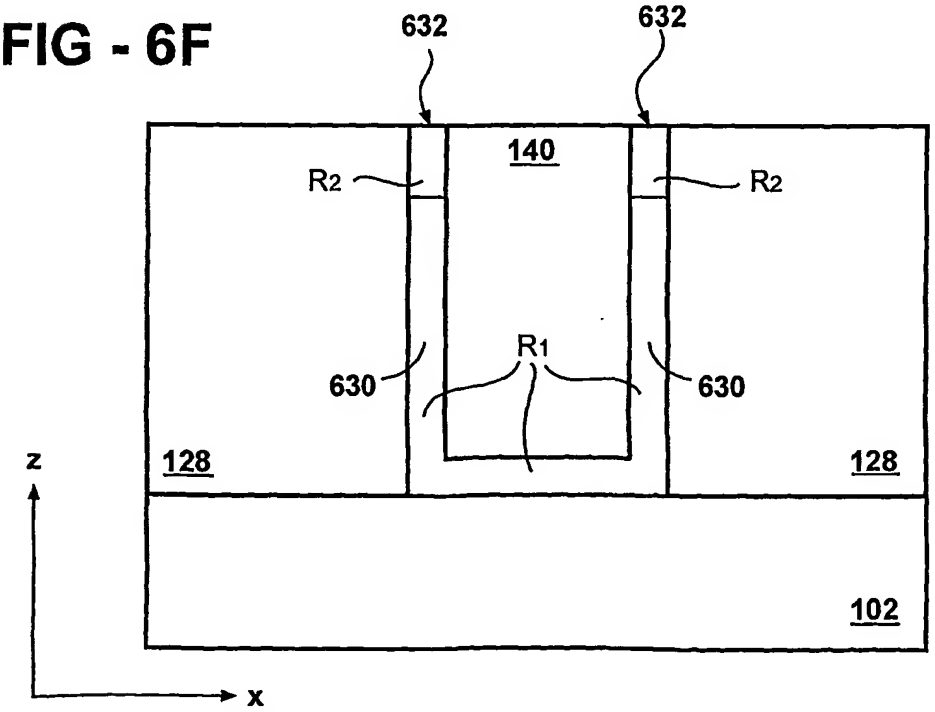

632
632
140
R2
R2
R1
630
630
128
128
102
z
x

FIG - 6G

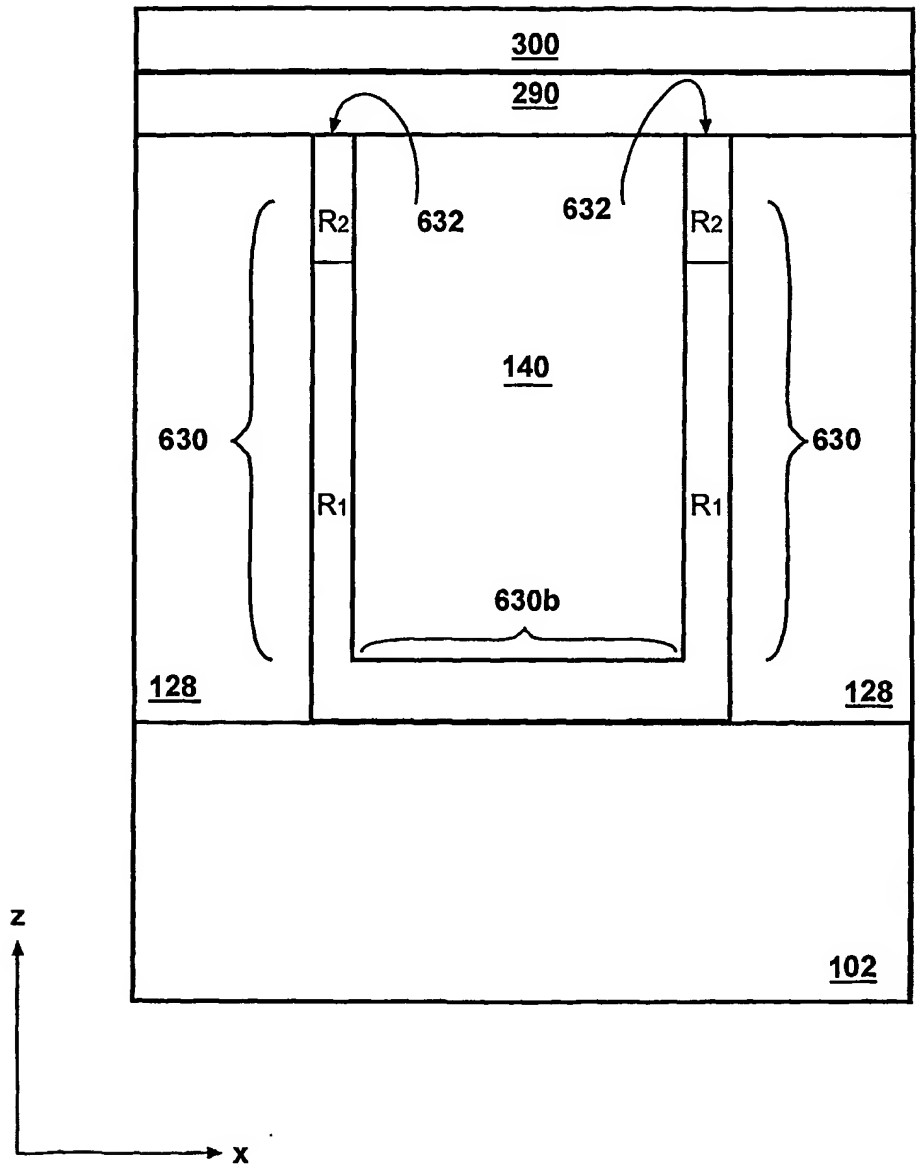


FIG - 7A

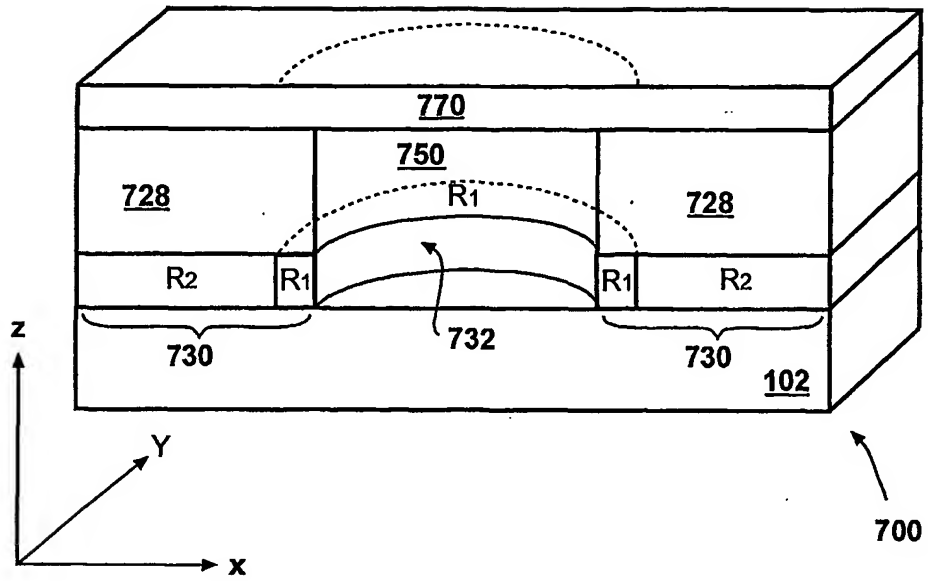

770
750
728
R1
728
R2
R1
R1
R2
730
732
730
102
z
Y
x
700

FIG - 7B

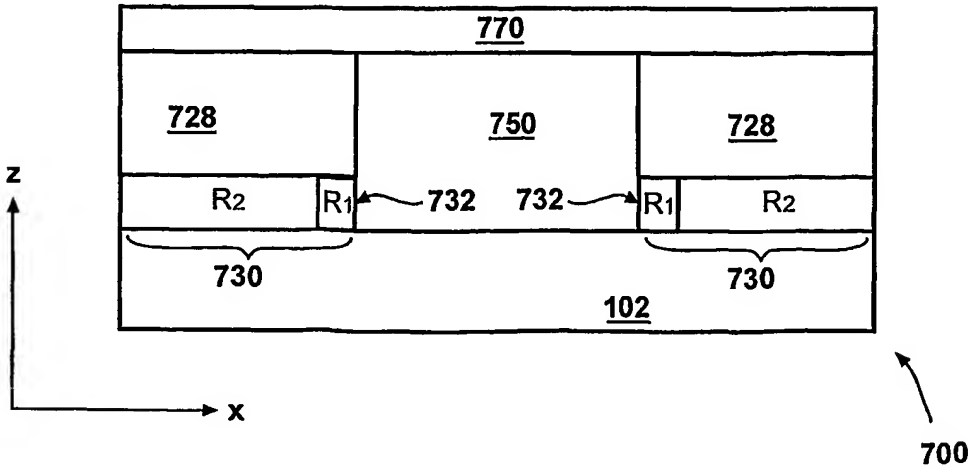

770
728
750
728
z
R2
R1
732
732
R1
R2
730
730
102
x
700

FIG - 8

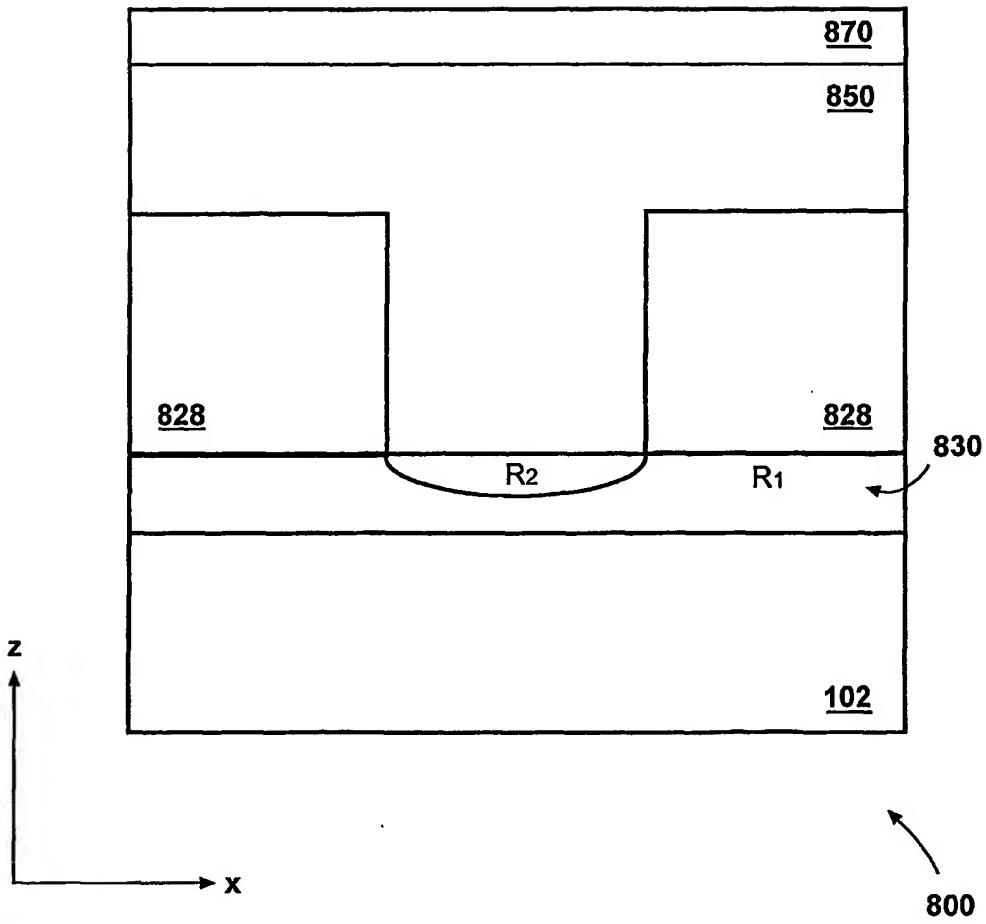


FIG - 9A

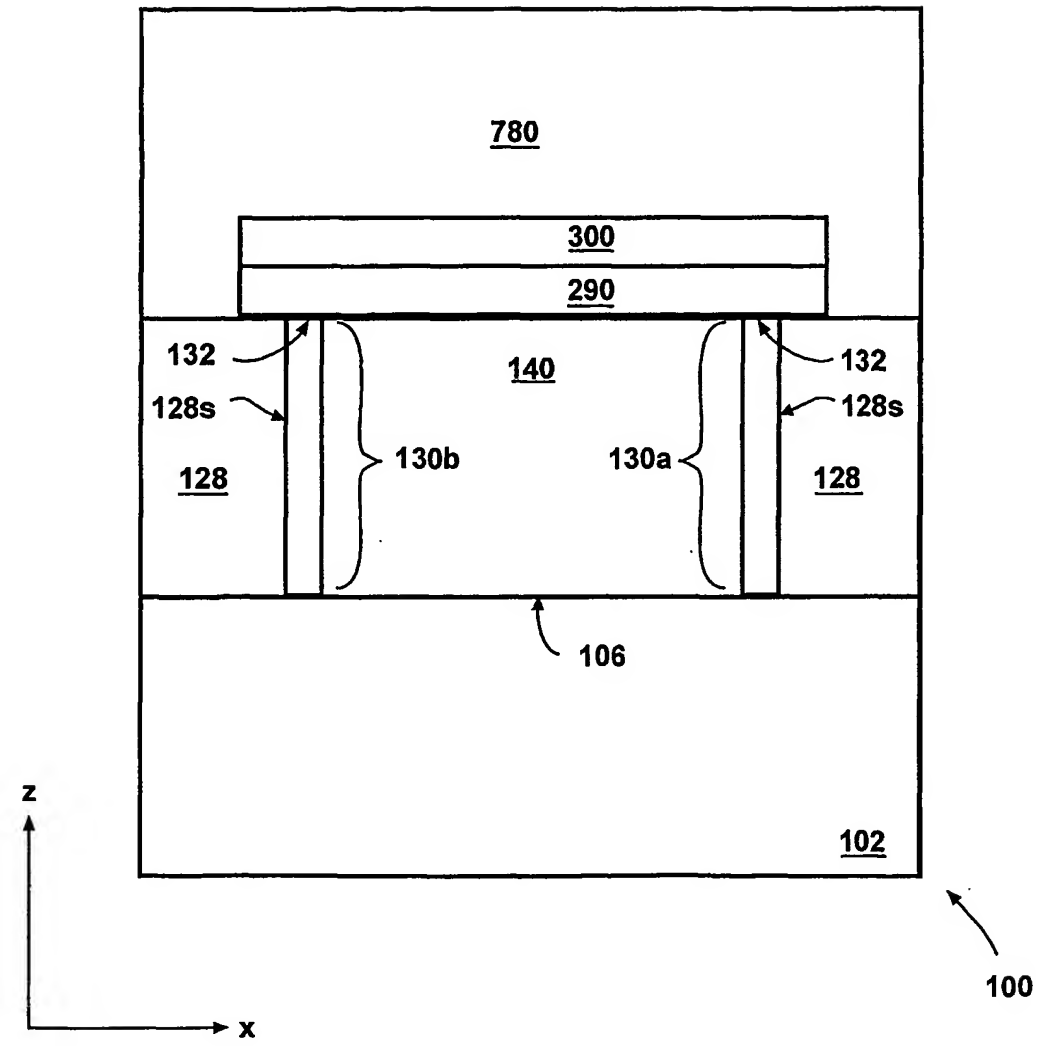

780
300
290
132
128s
128
140
130b
130a
132
128s
128
106
102
100
z
x

FIG - 9B

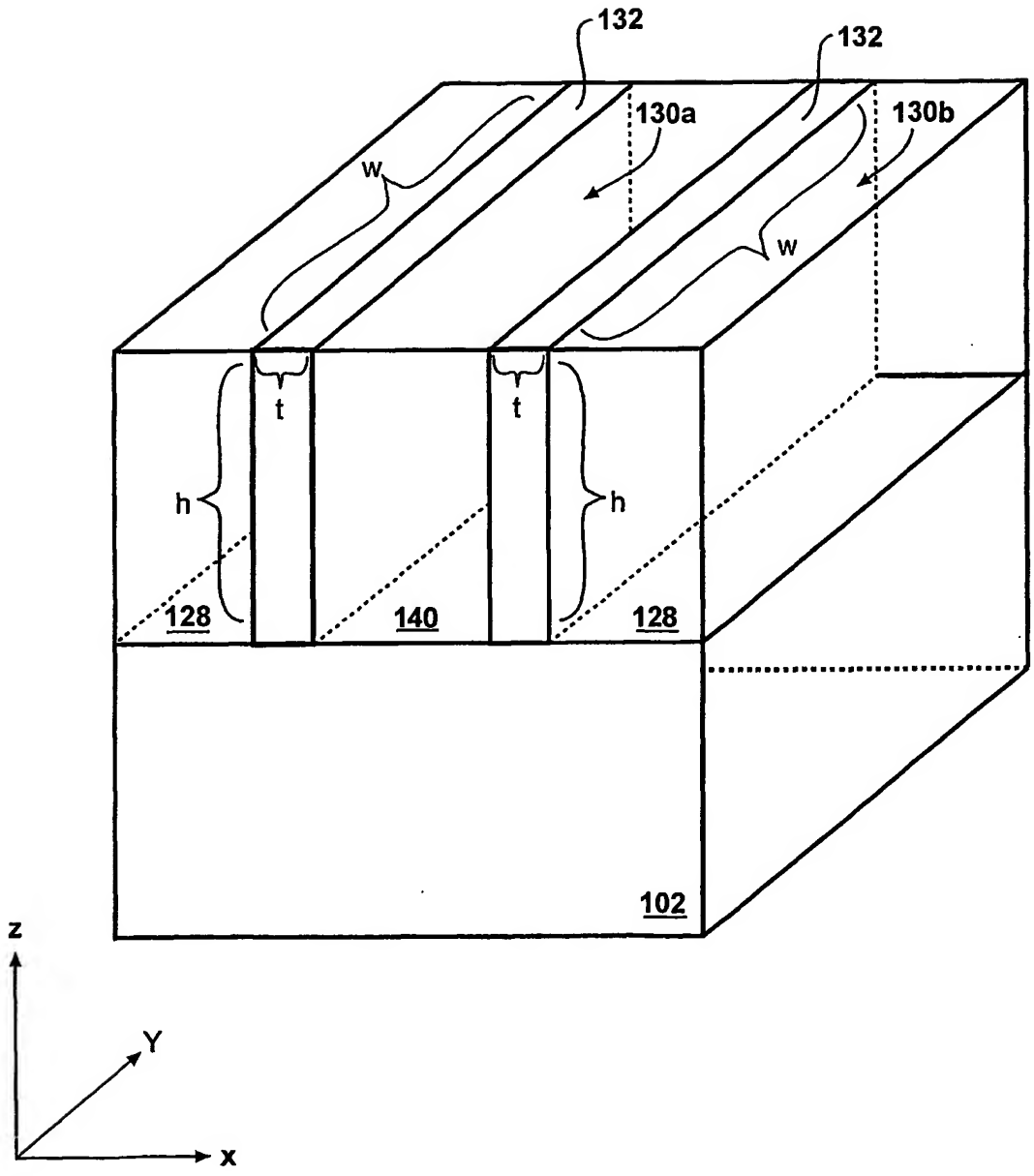


FIG - 9C

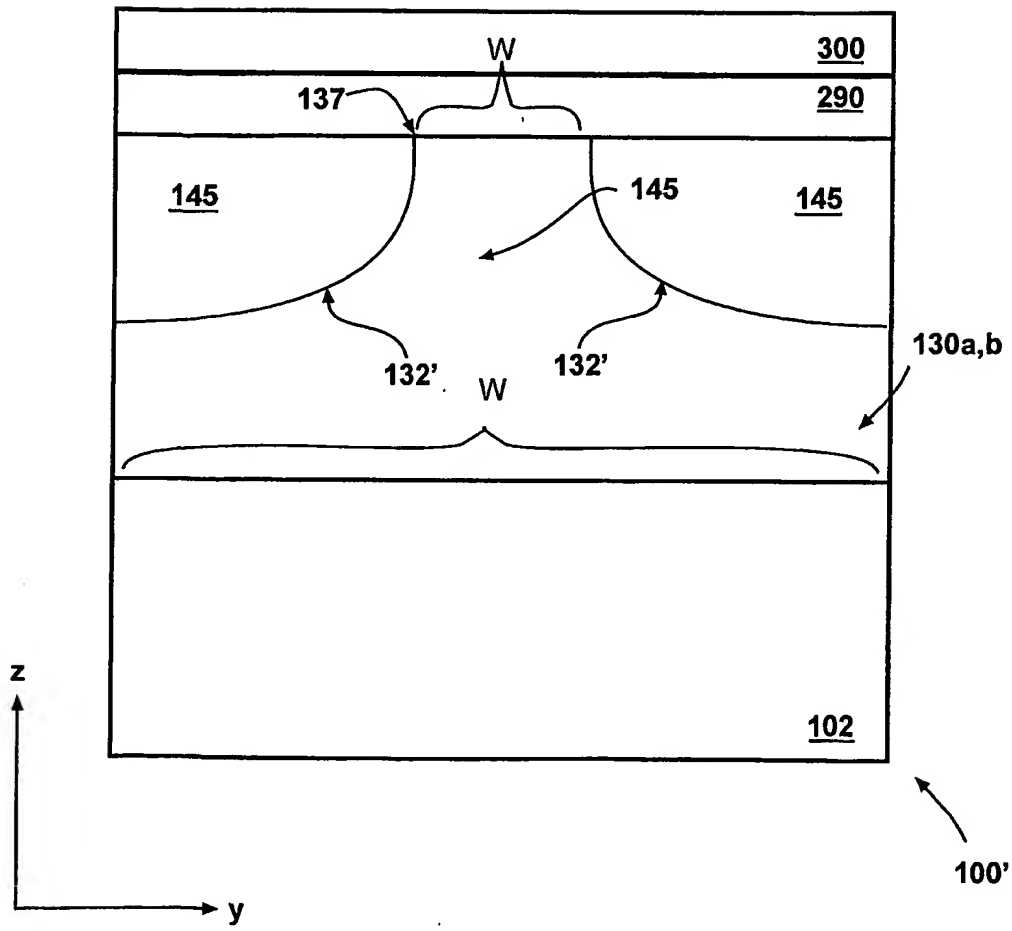


FIG - 9D

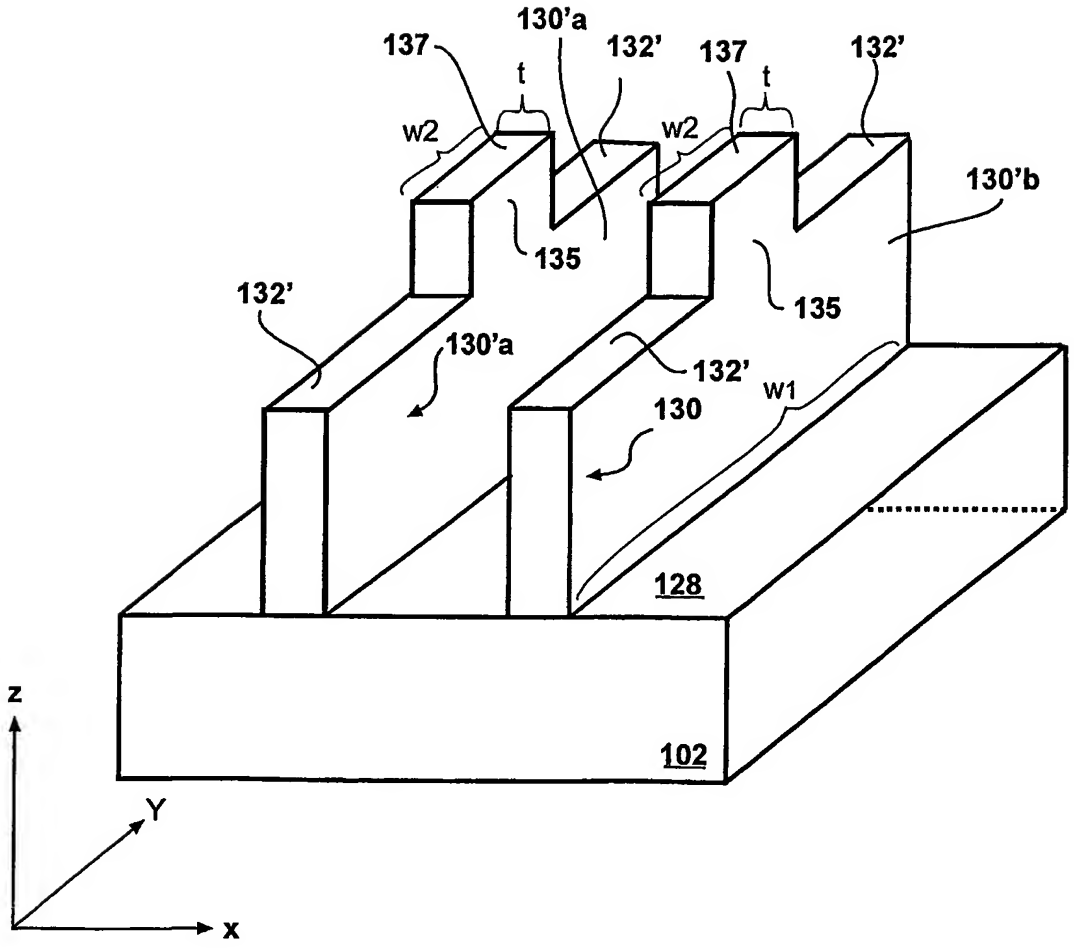

137
130'a
132'
137
132'
t
t
w2
w2
130'b
135
135
132'
130'a
132'
130
w1
128
102
z
Y
x

FIG - 10A

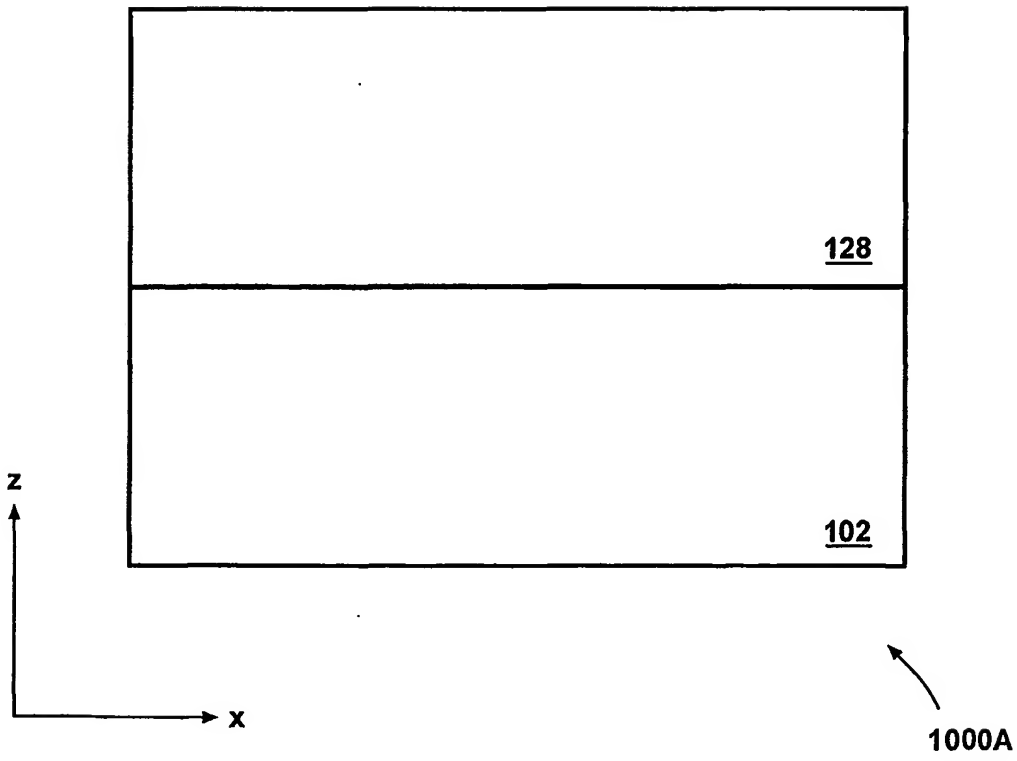


FIG - 10B

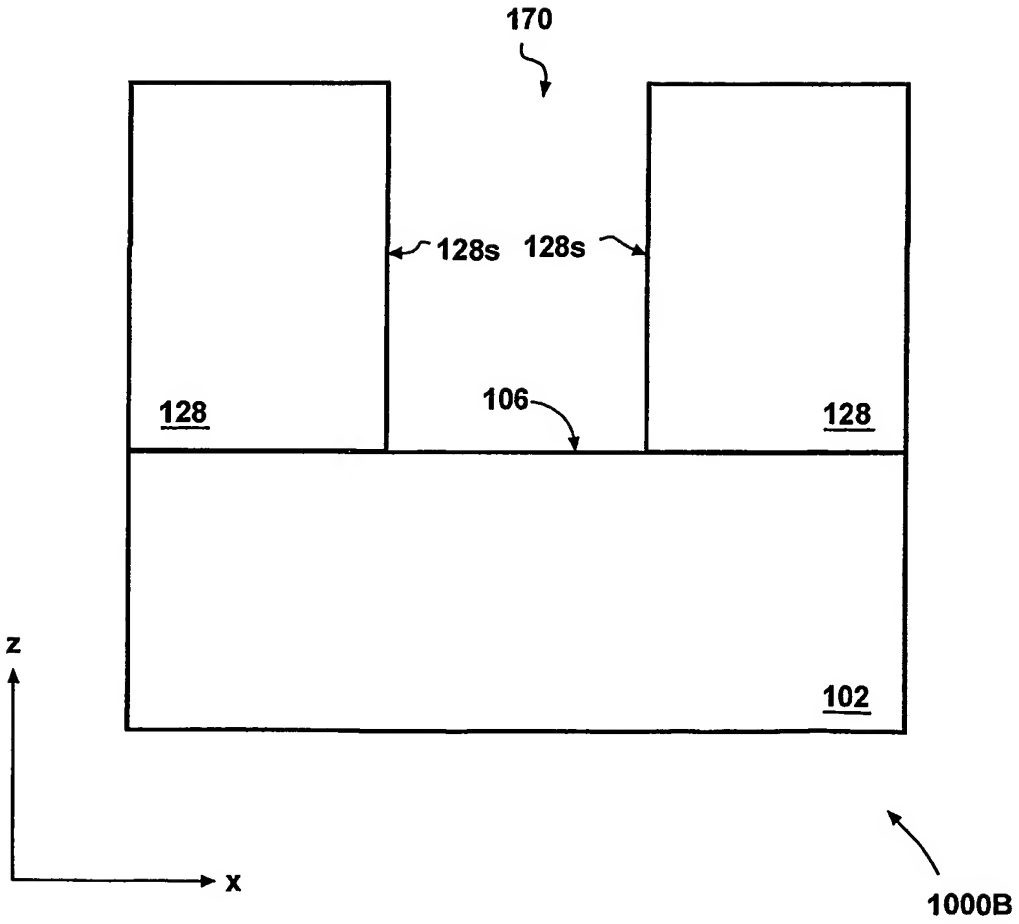


FIG - 10C

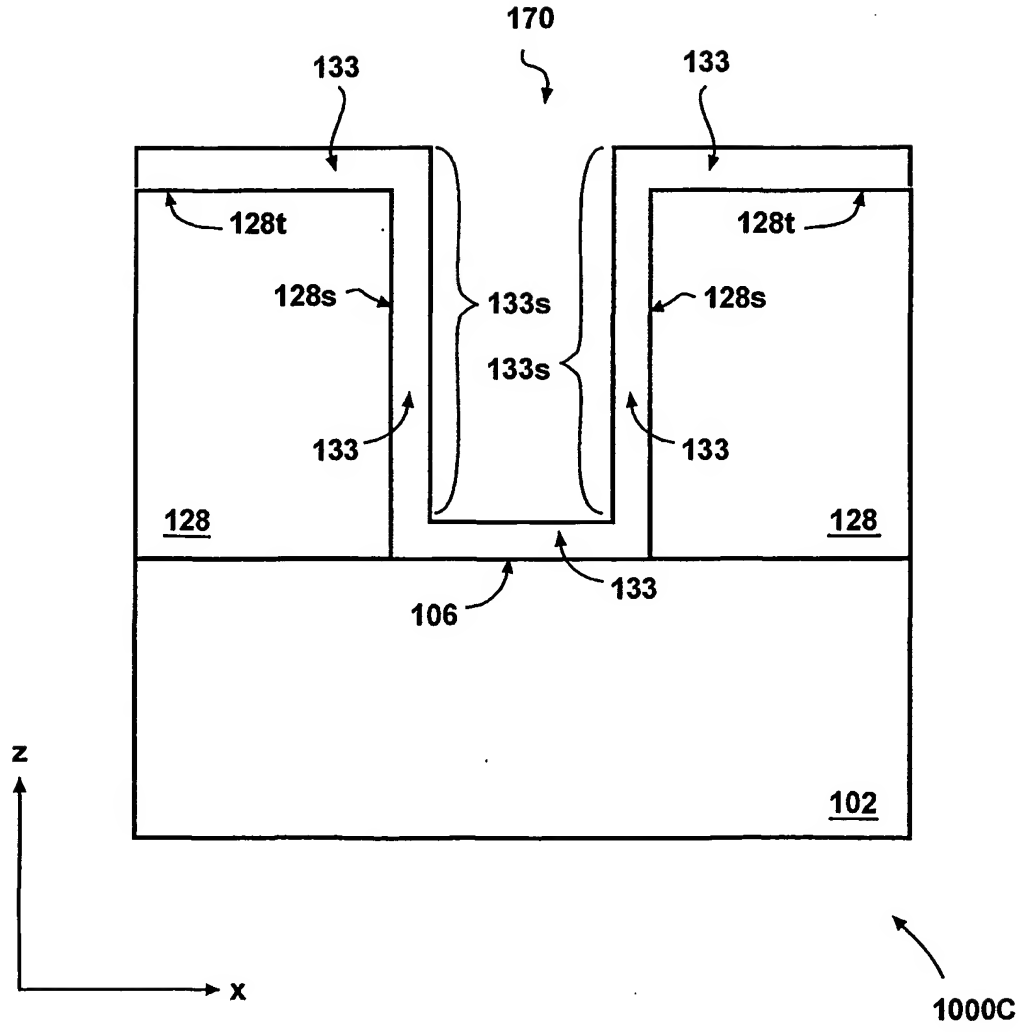

170
133
133
128t
128t
128s
133s
128s
133s
133
133
128
128
106
133
102
z
x
1000C

FIG - 10D

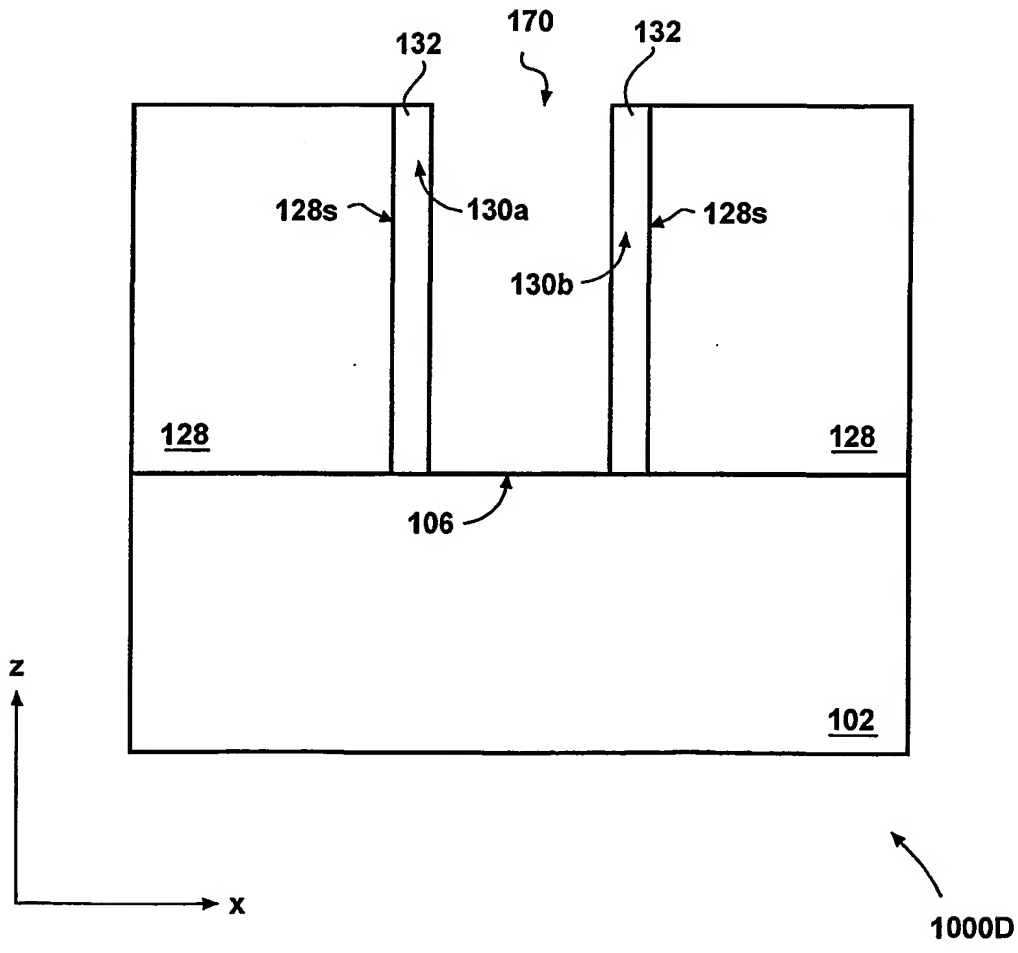


FIG - 10E

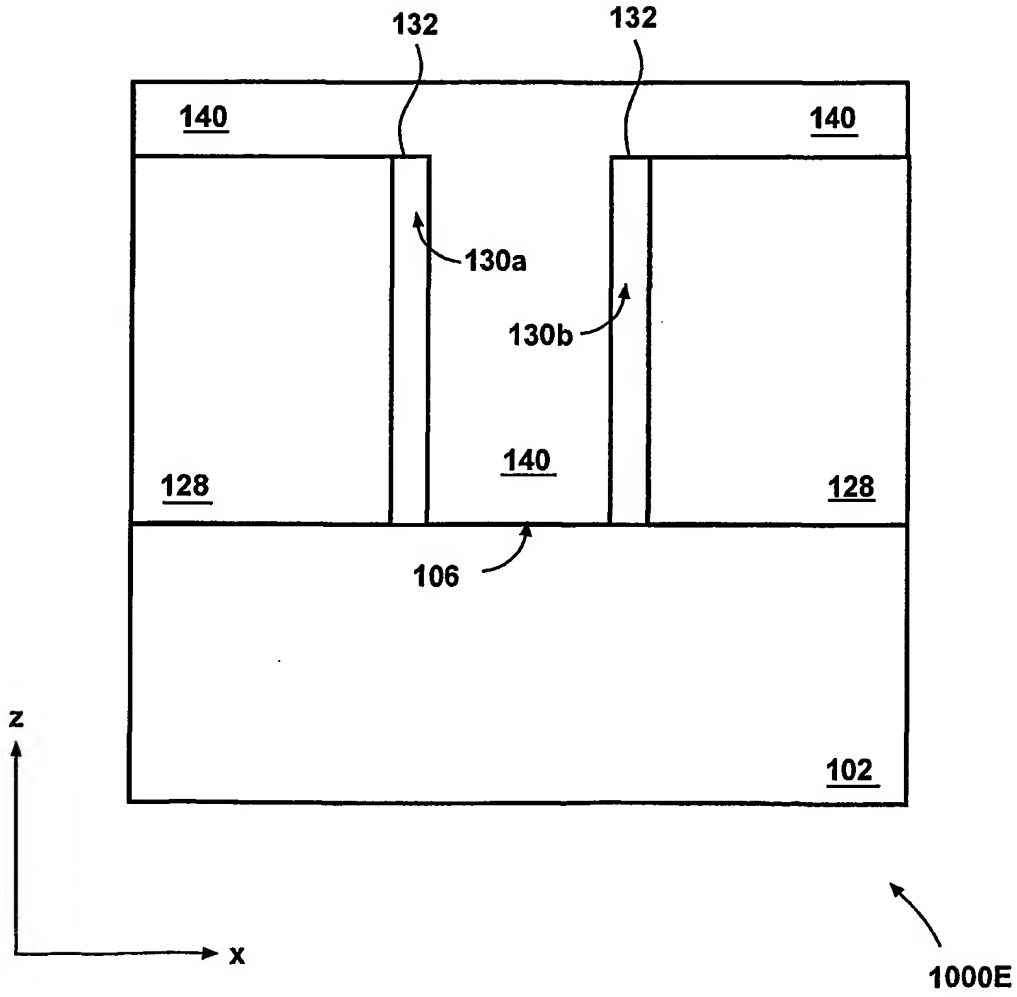


FIG - 10F

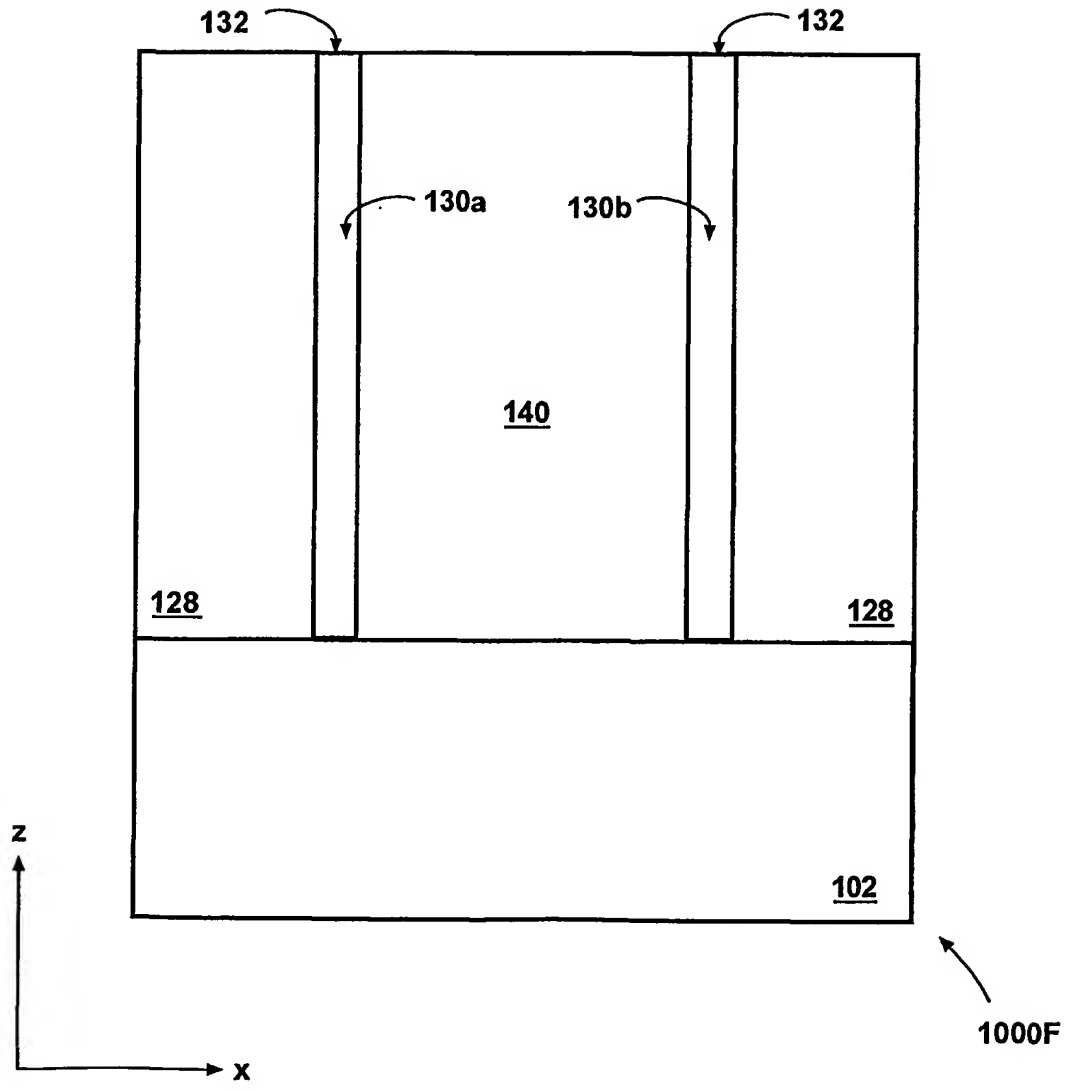


FIG - 10F'

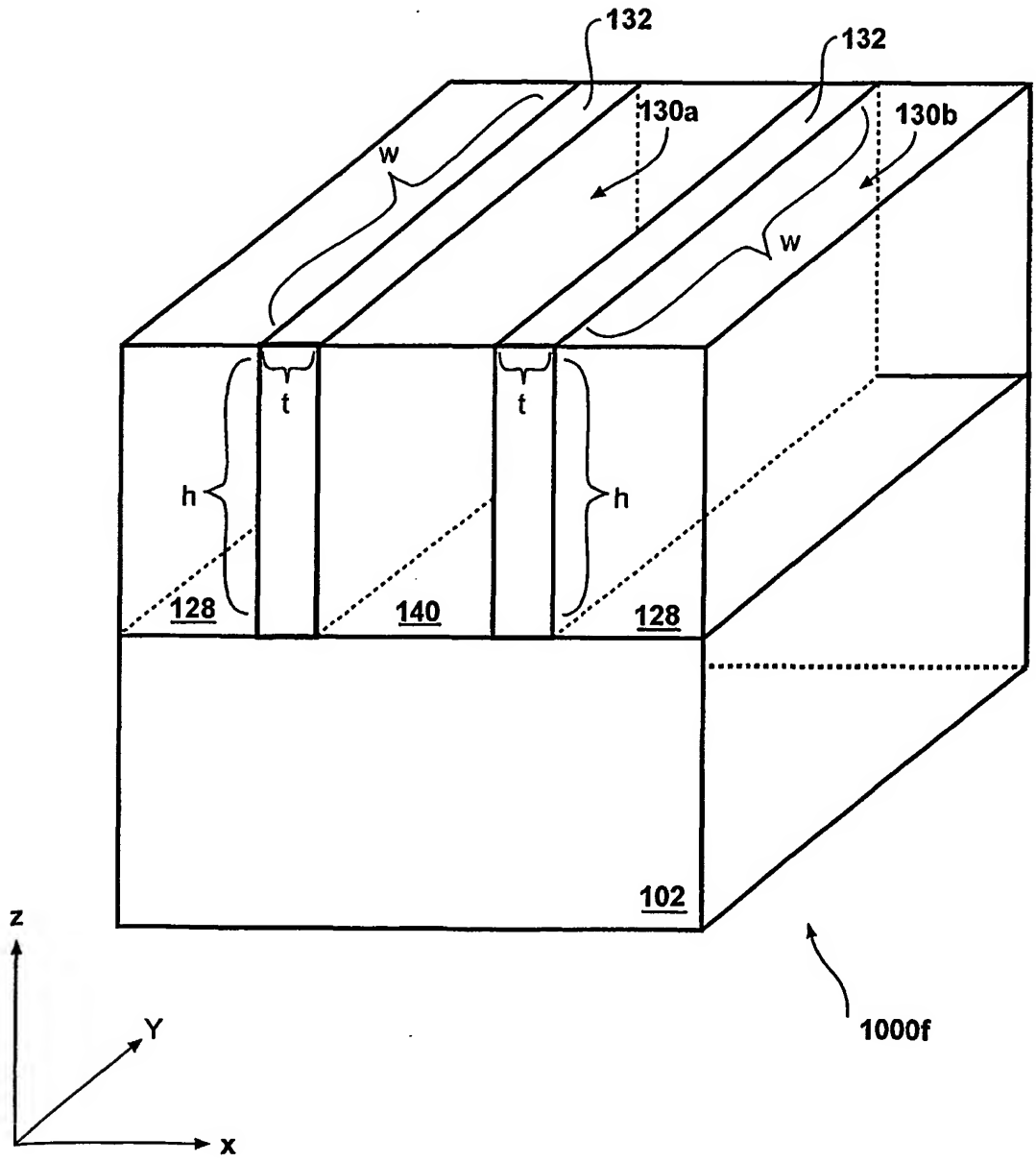


FIG - 10G

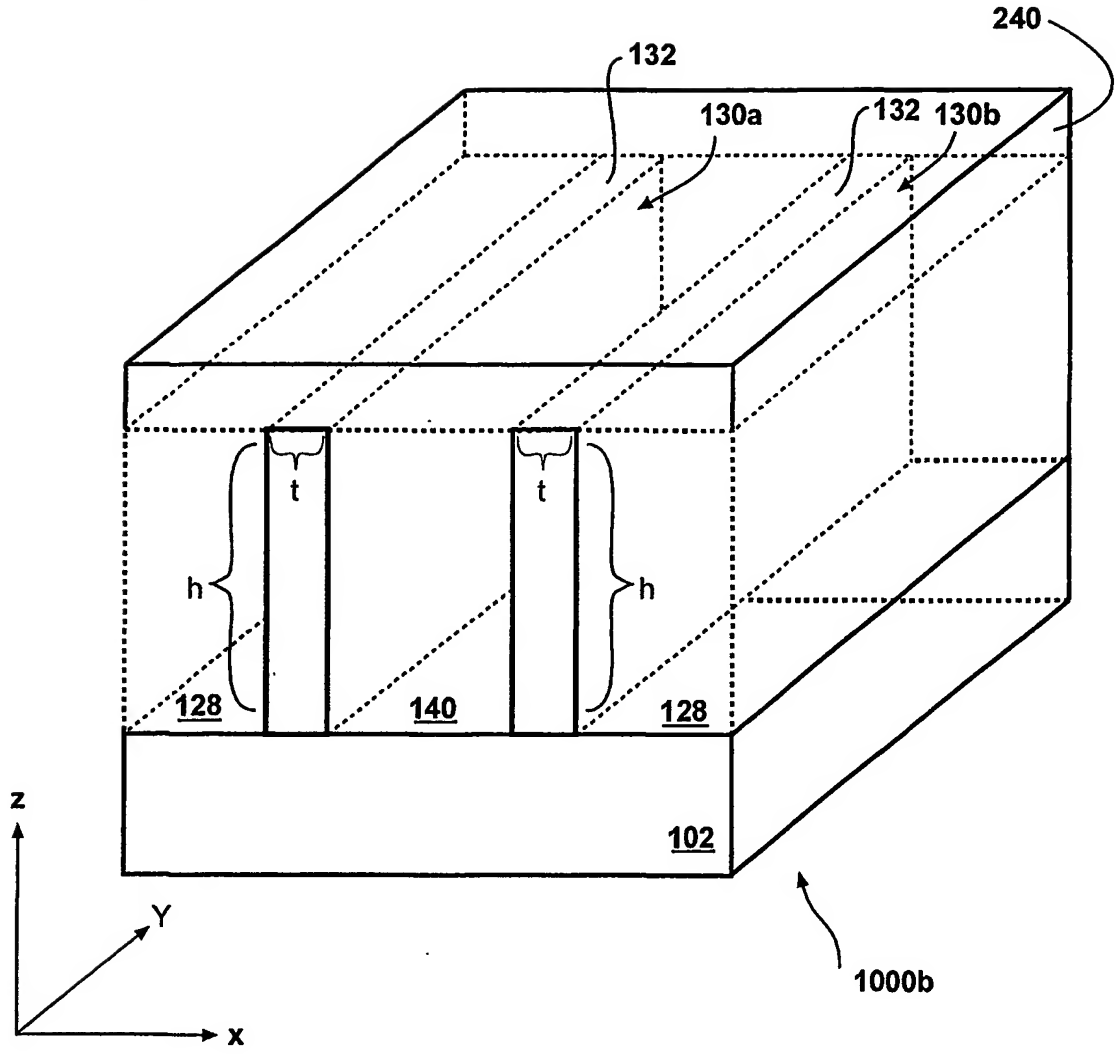


FIG - 10G'

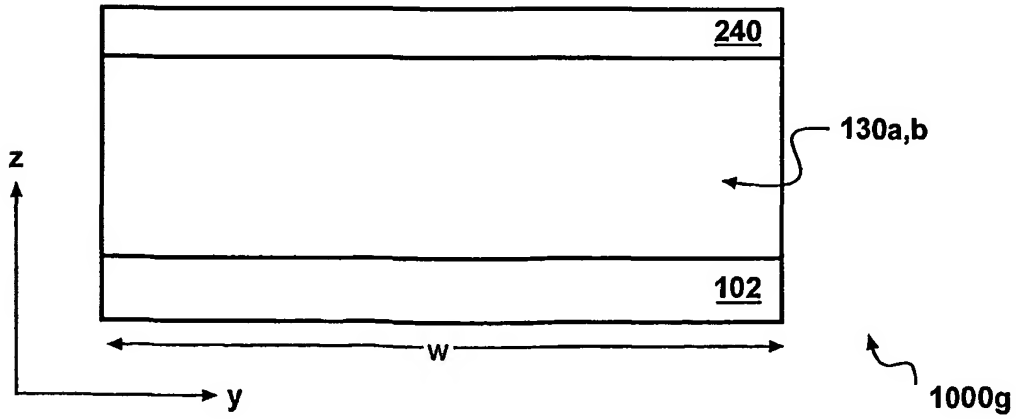


FIG - 10H'

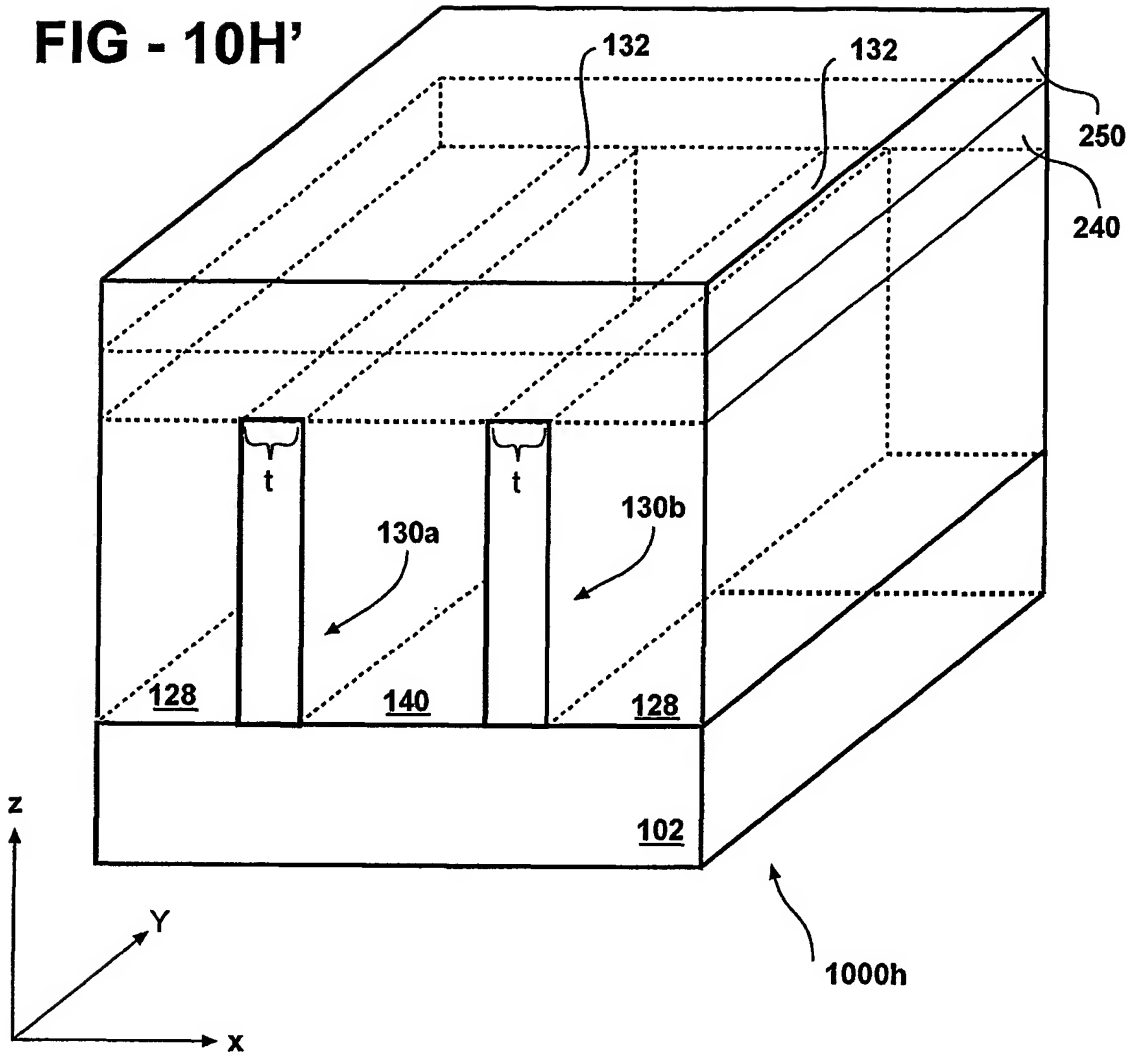


FIG - 10H

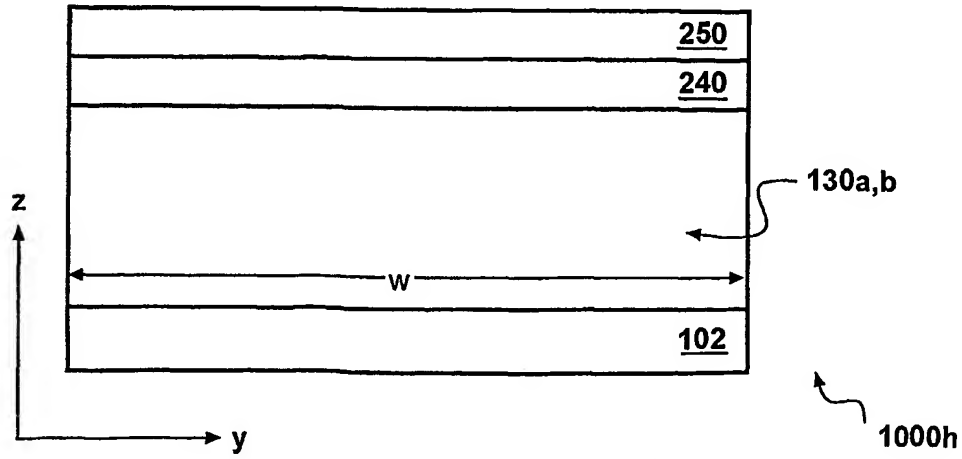


FIG - 10I

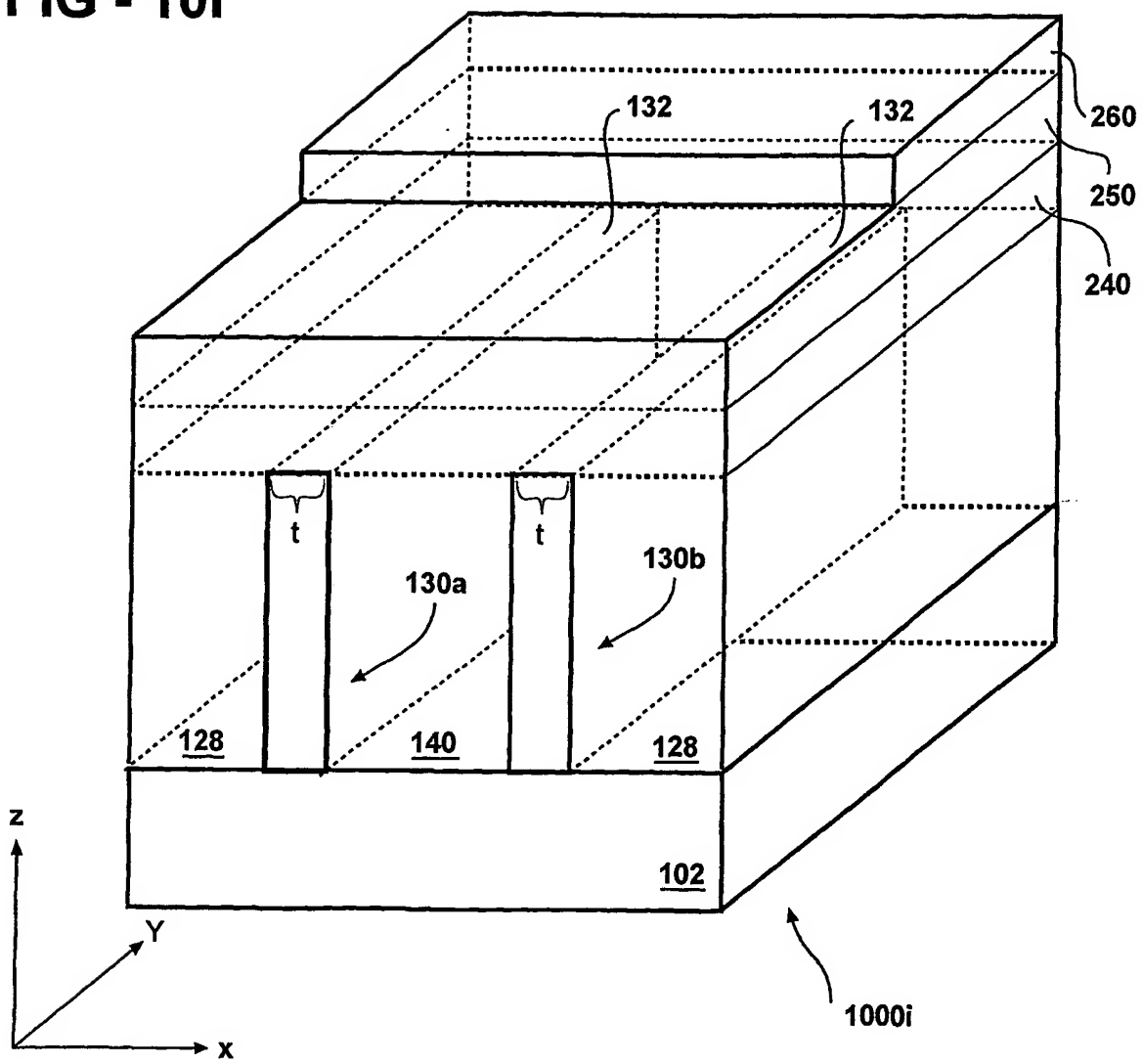


FIG - 10I'

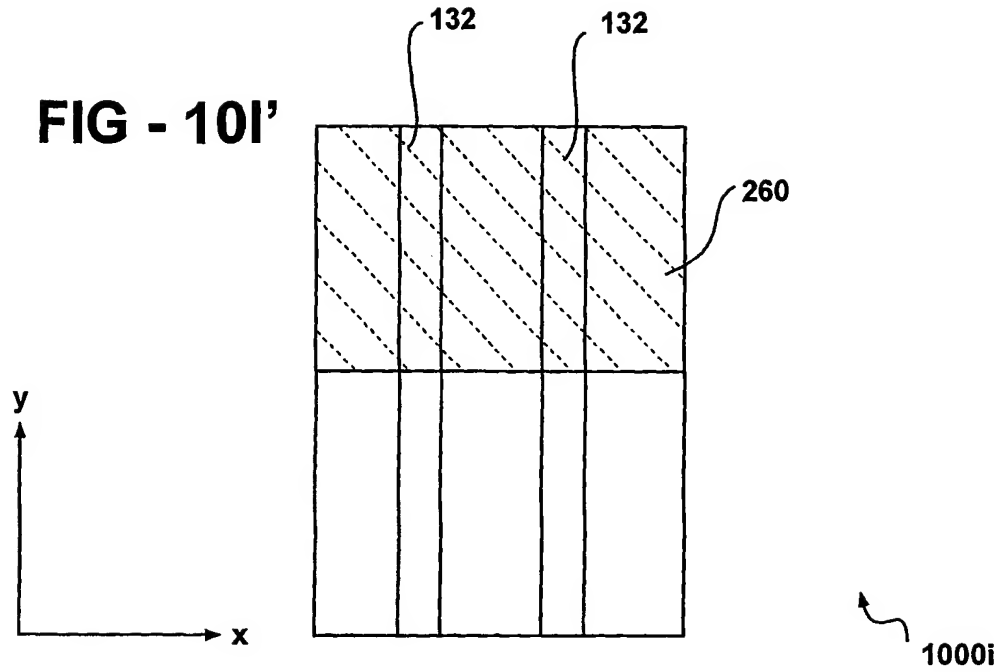


FIG - 10I"

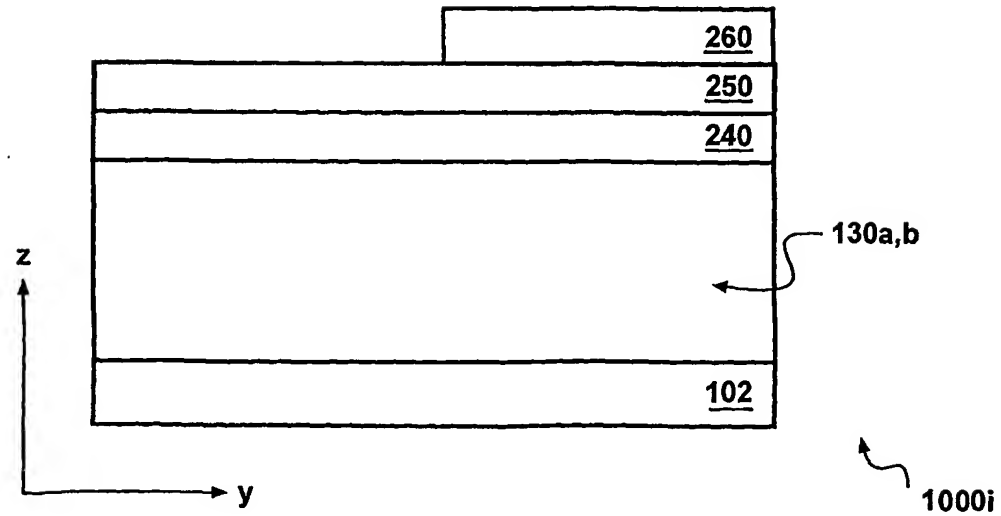


FIG - 10J

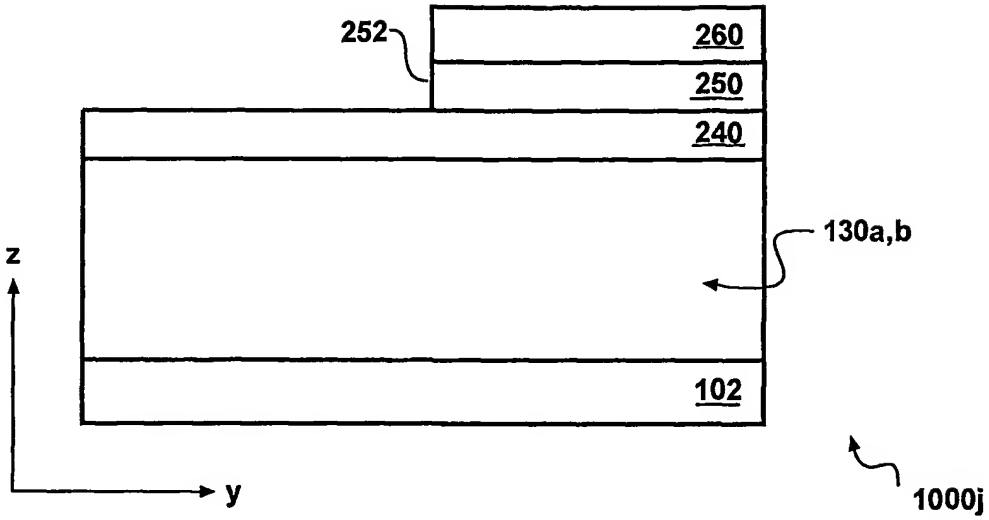
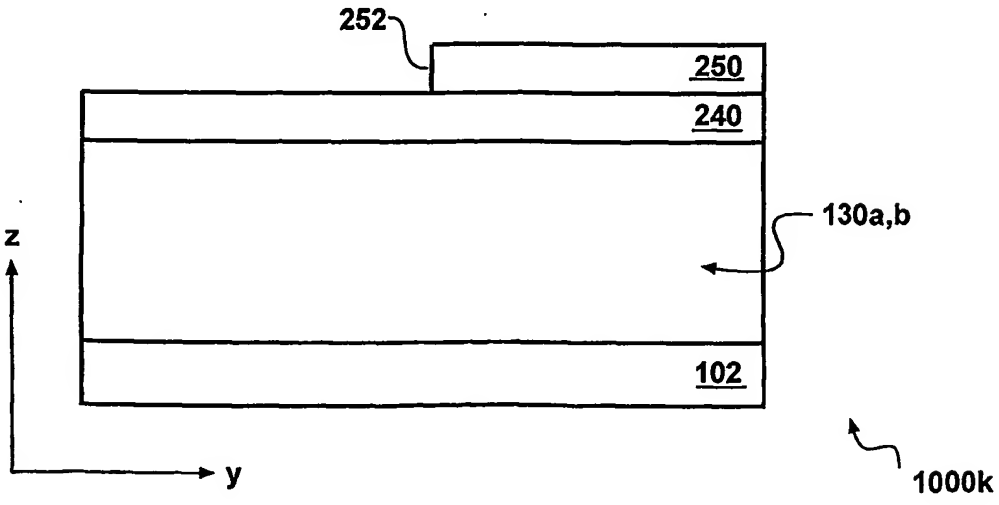


FIG - 10K



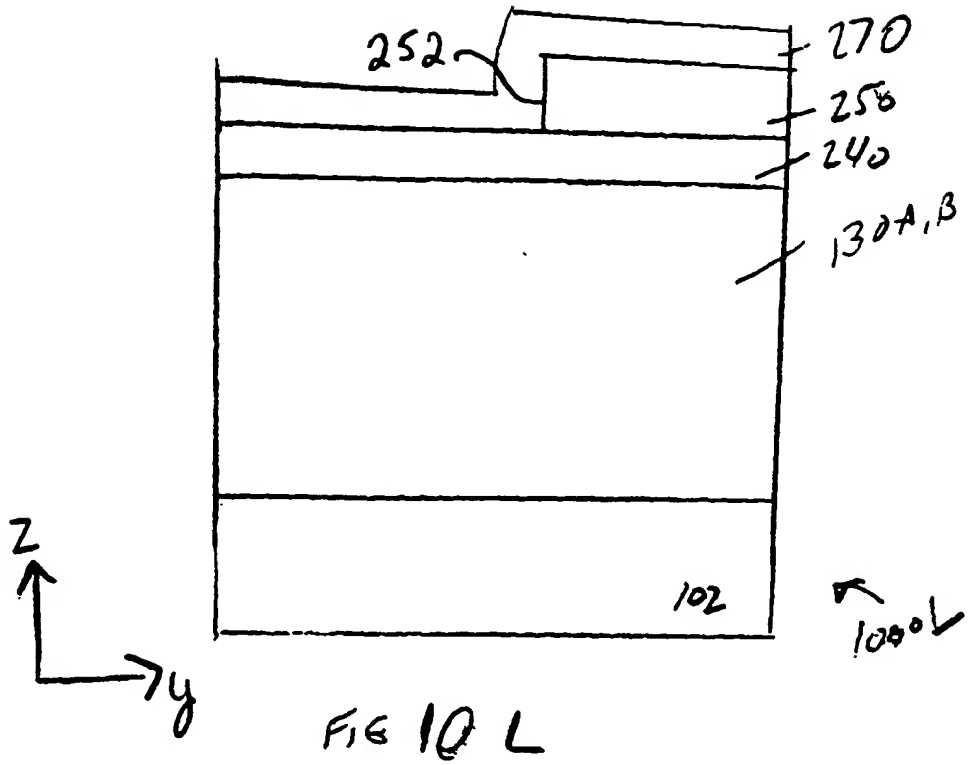


FIG 10L

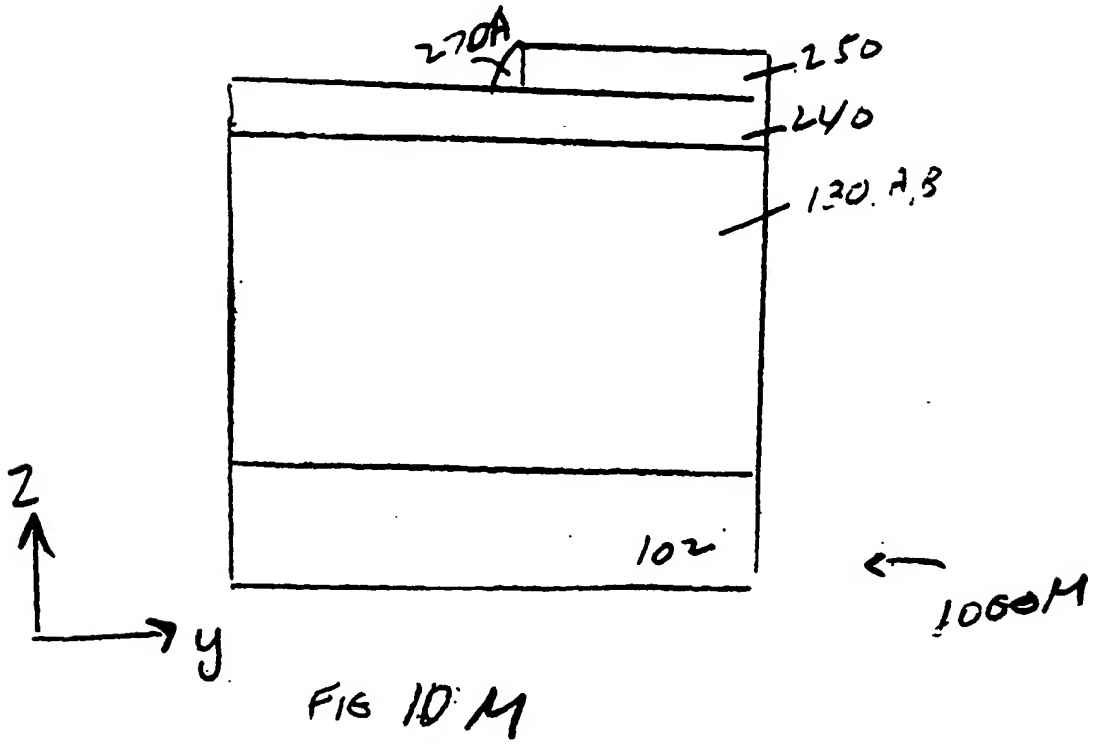


FIG 10M

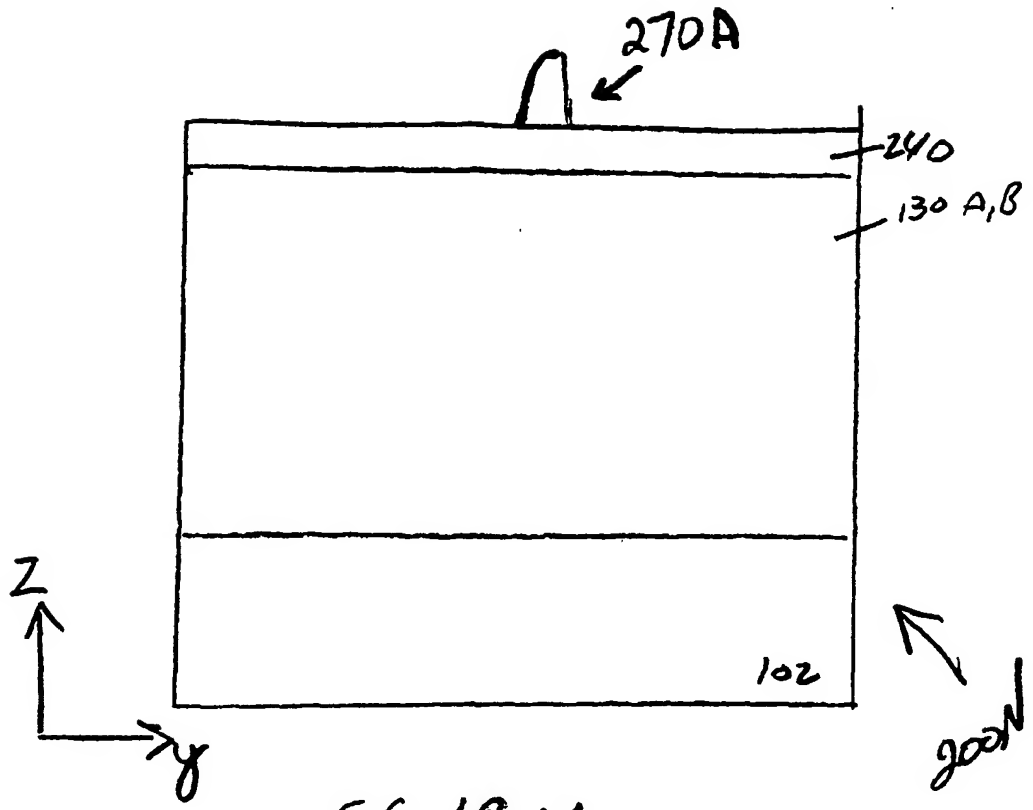


FIG 10.N

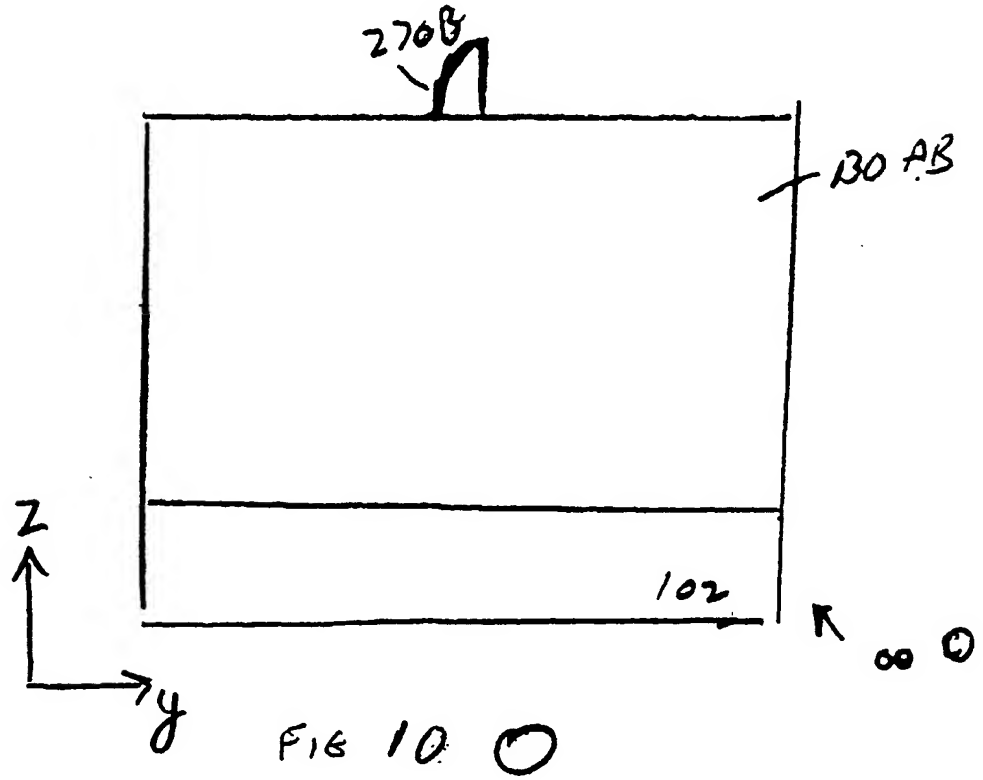


FIG 10 O

FIG - 10O'

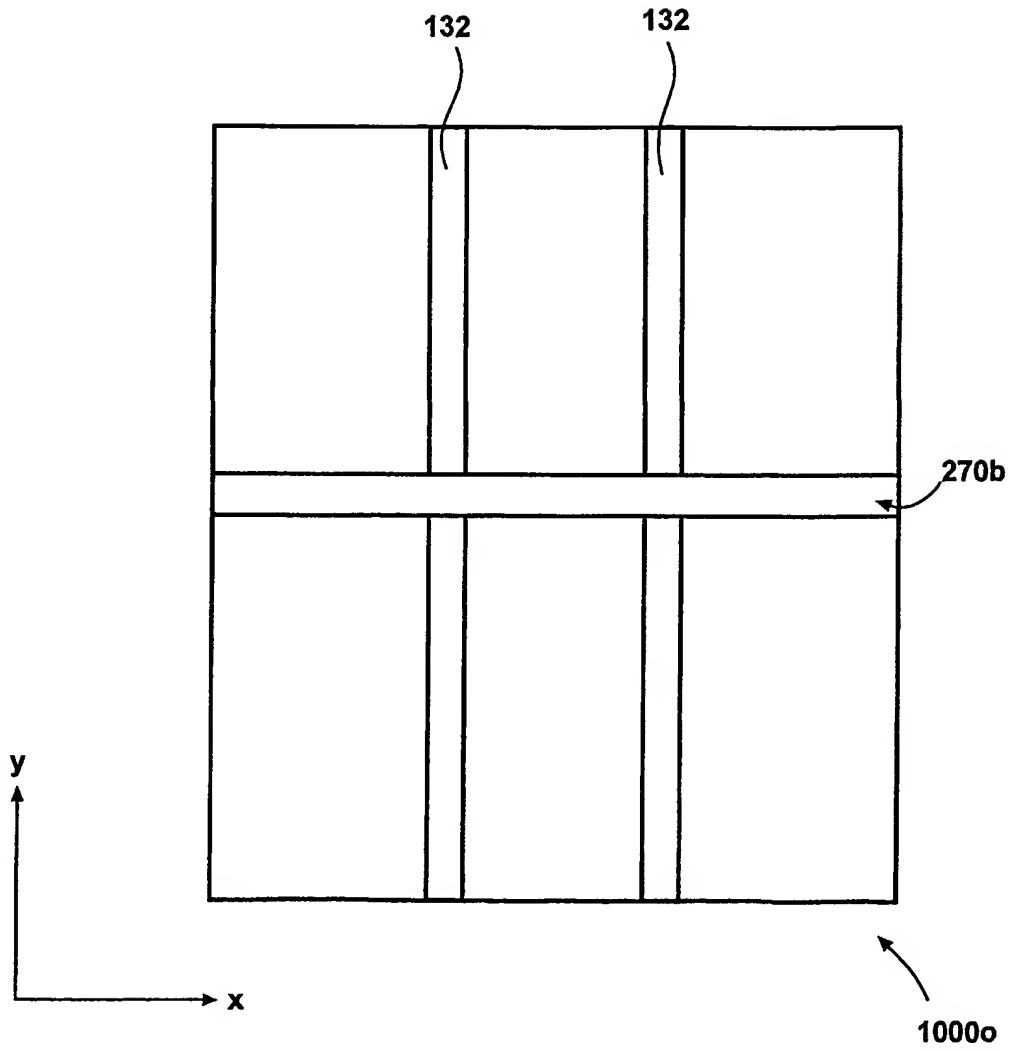


FIG - 10O"

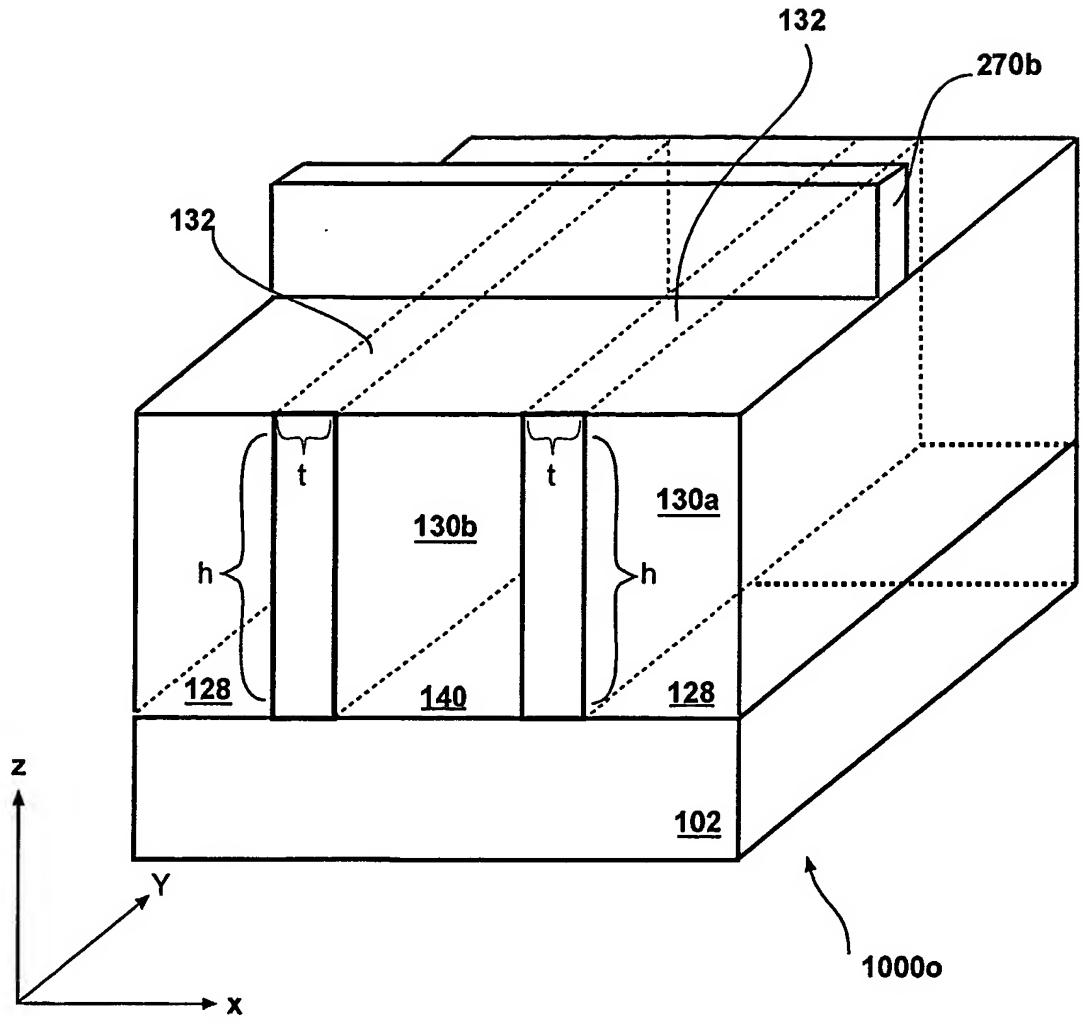


FIG - 10P

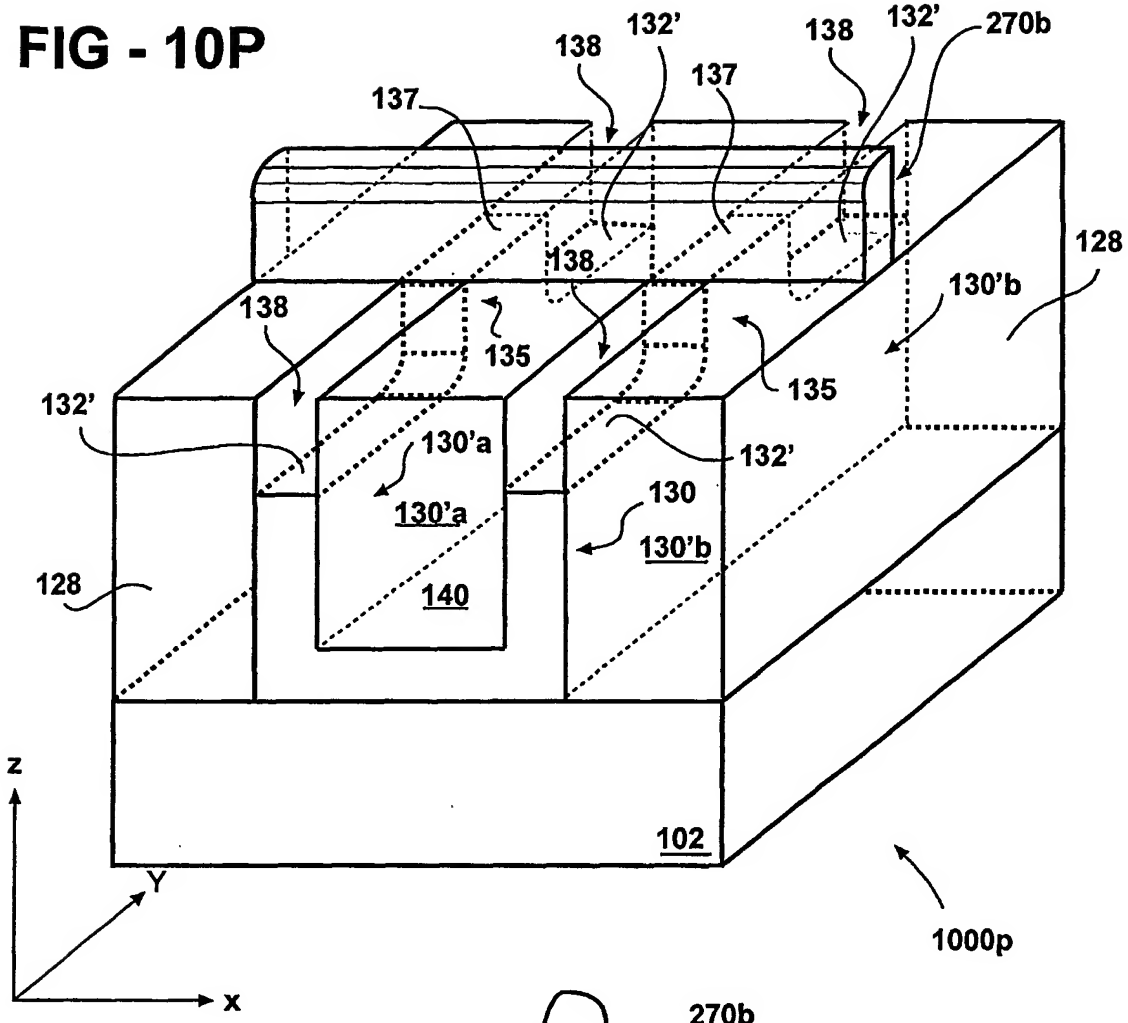


FIG - 10P'

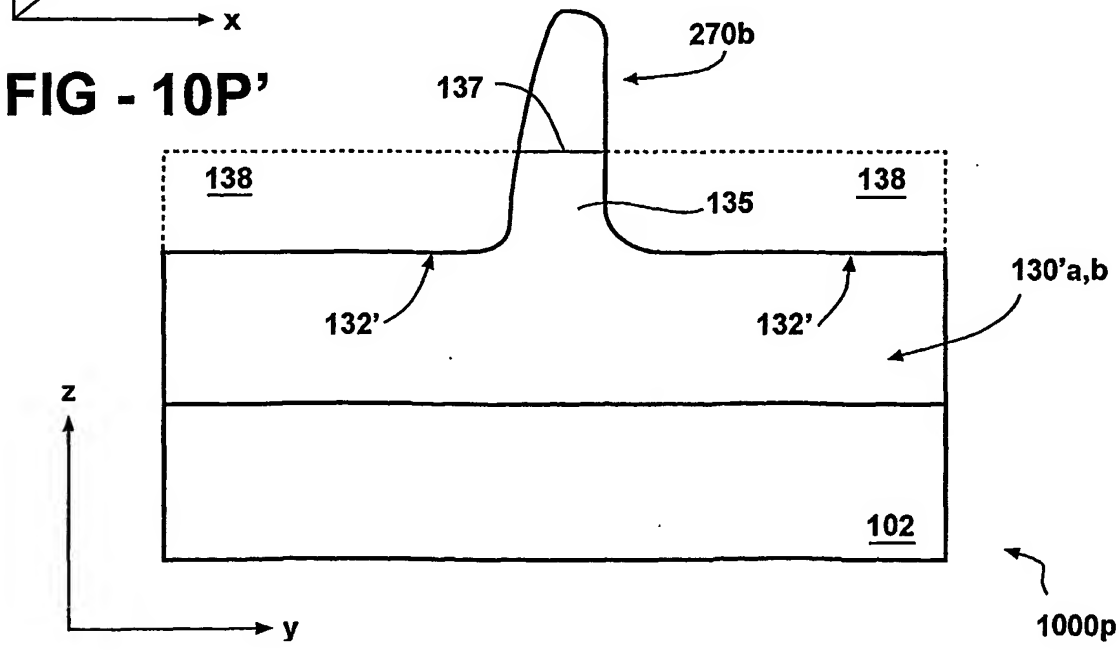


FIG - 10Q

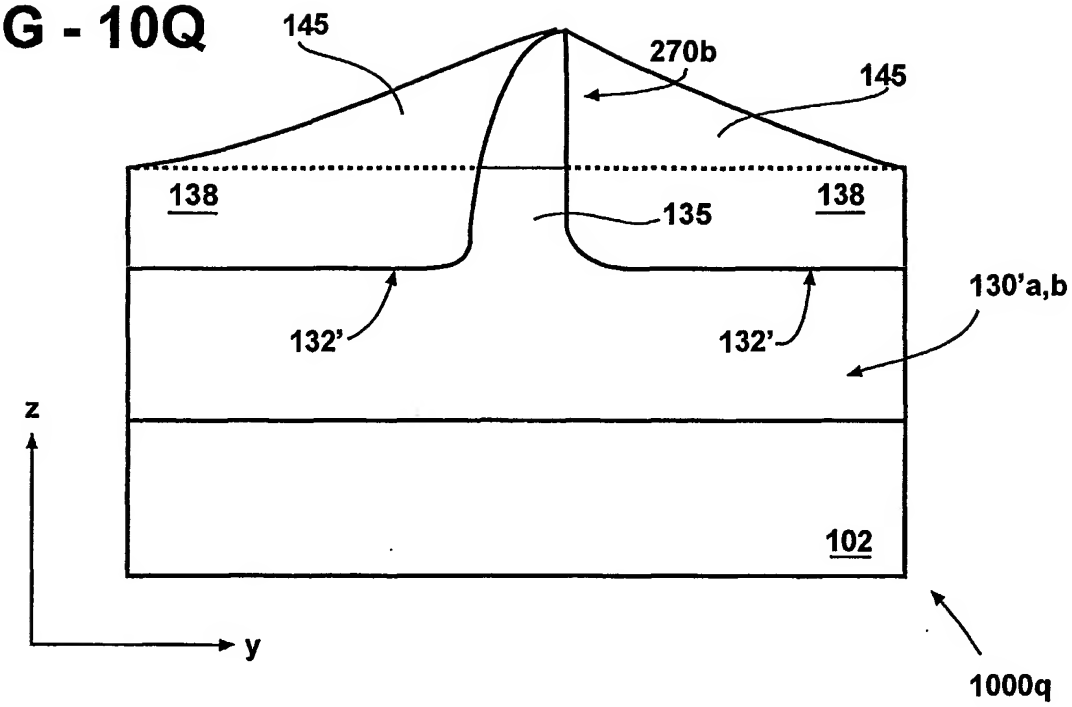


FIG - 10R

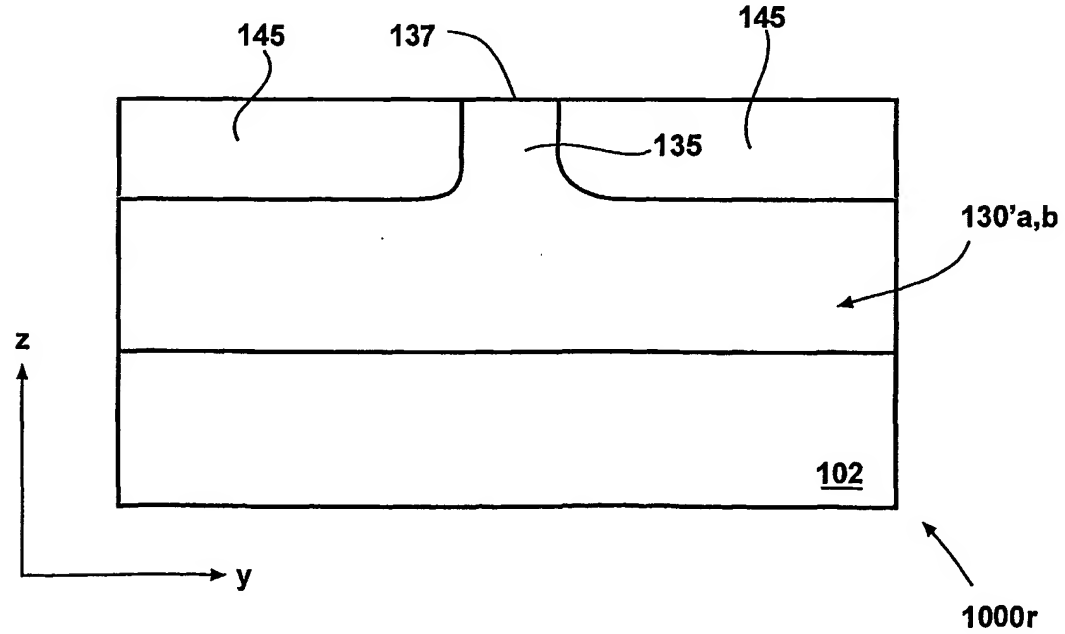


FIG - 10S

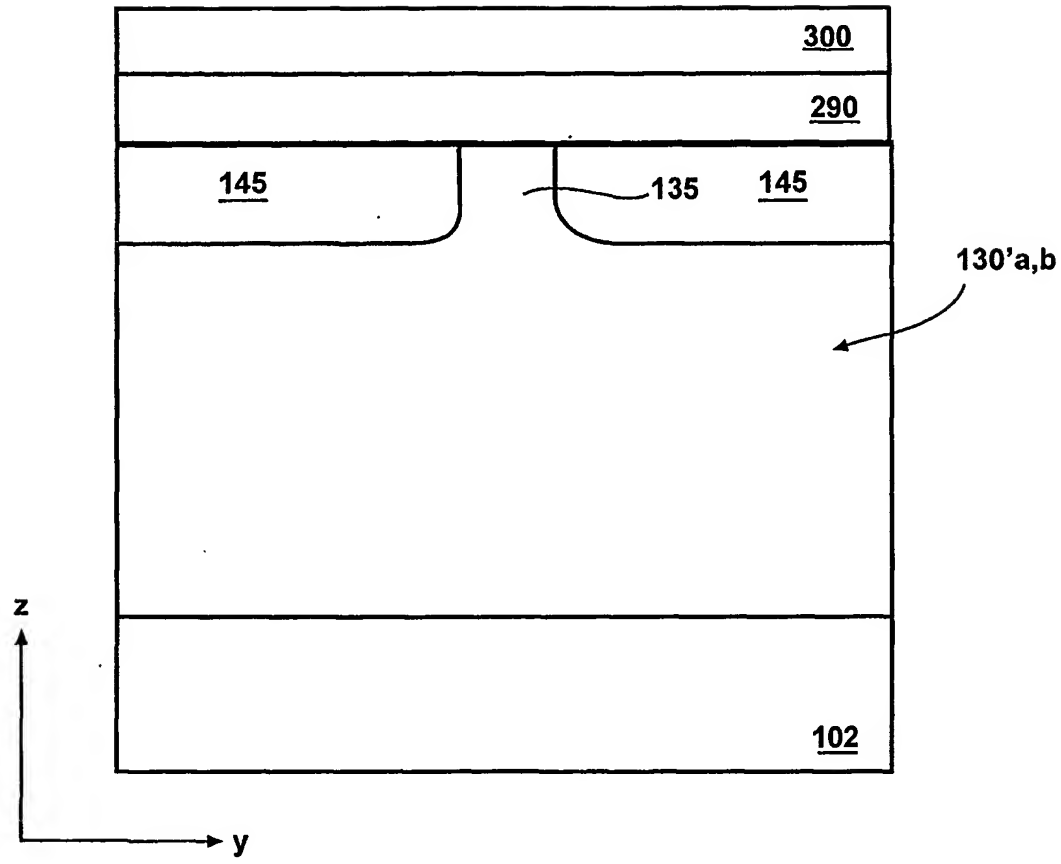


FIG - 11

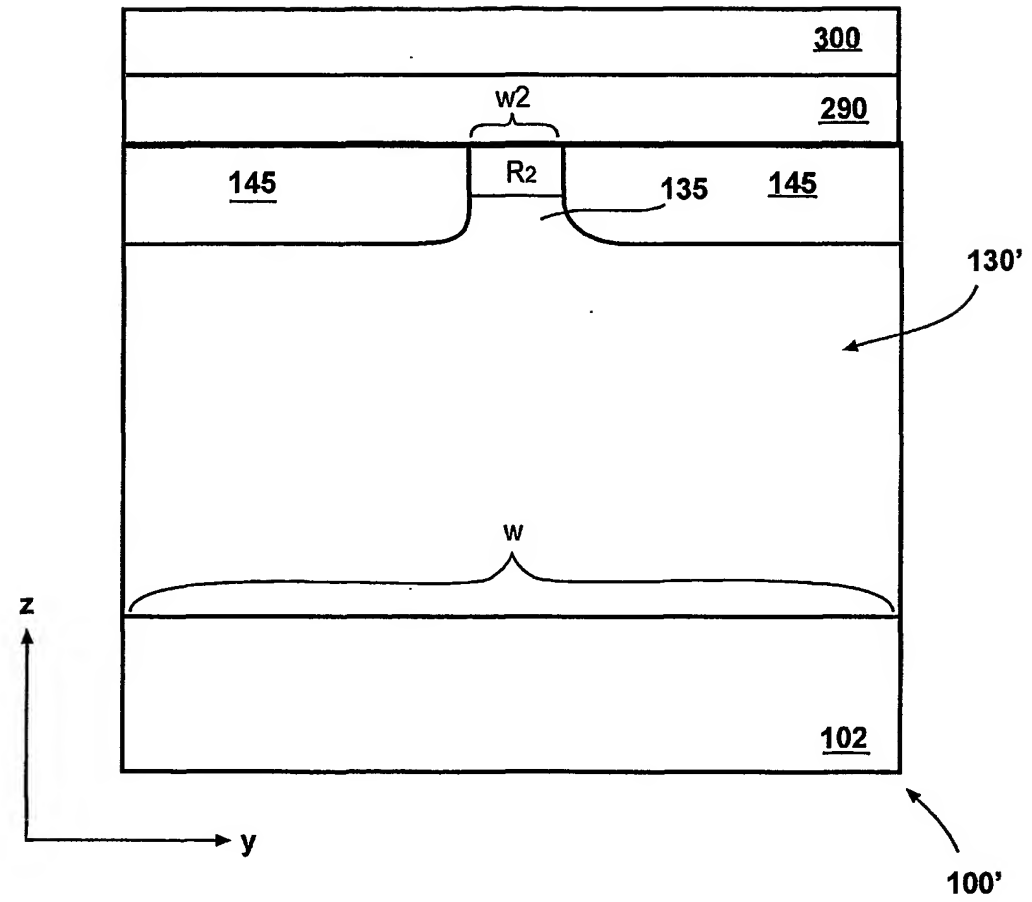


FIG - 12A

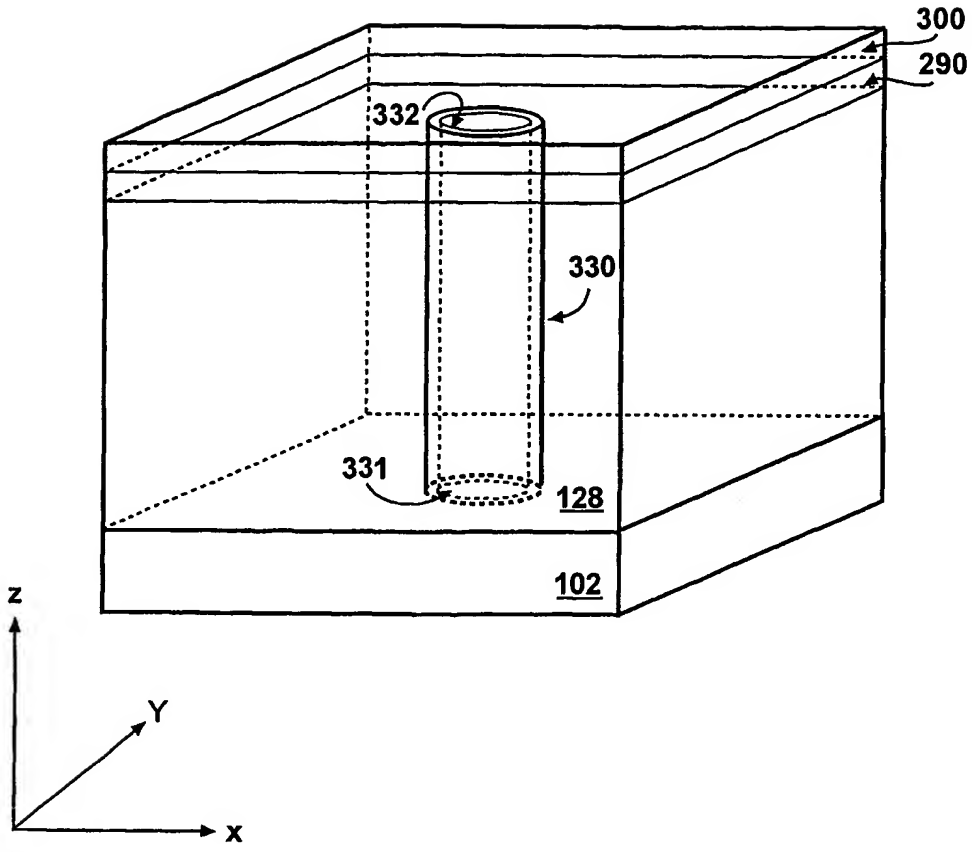


FIG - 12B

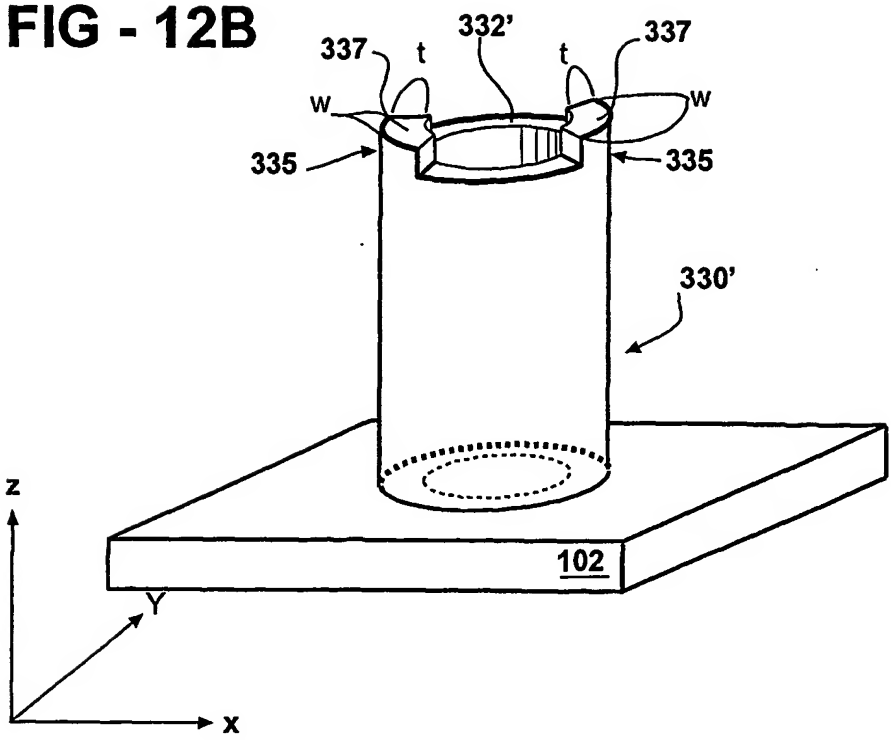


FIG - 12C

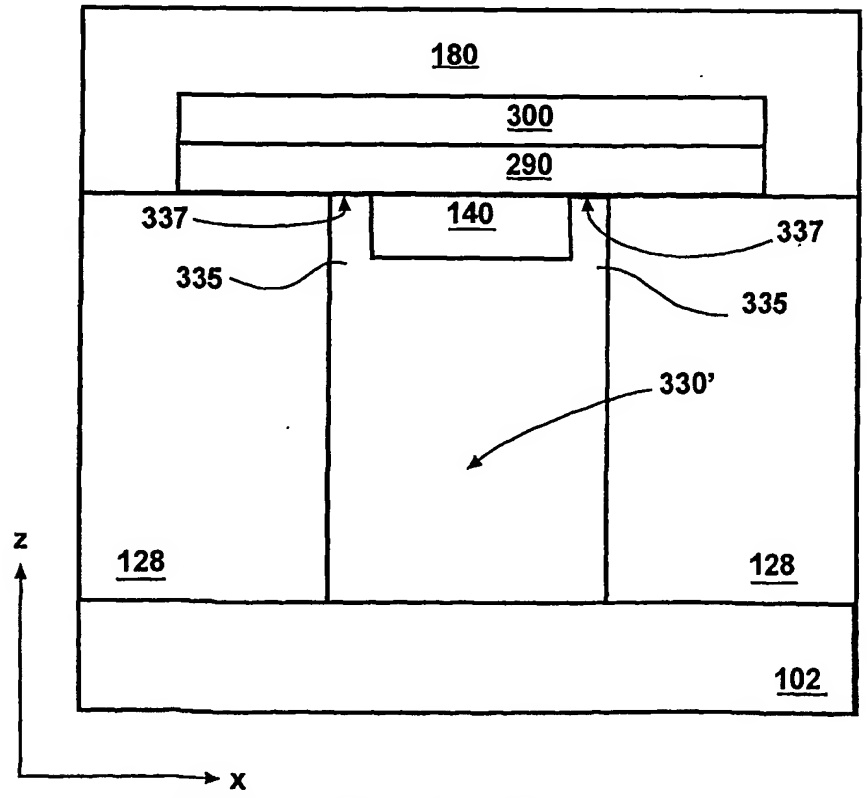


FIG - 13A

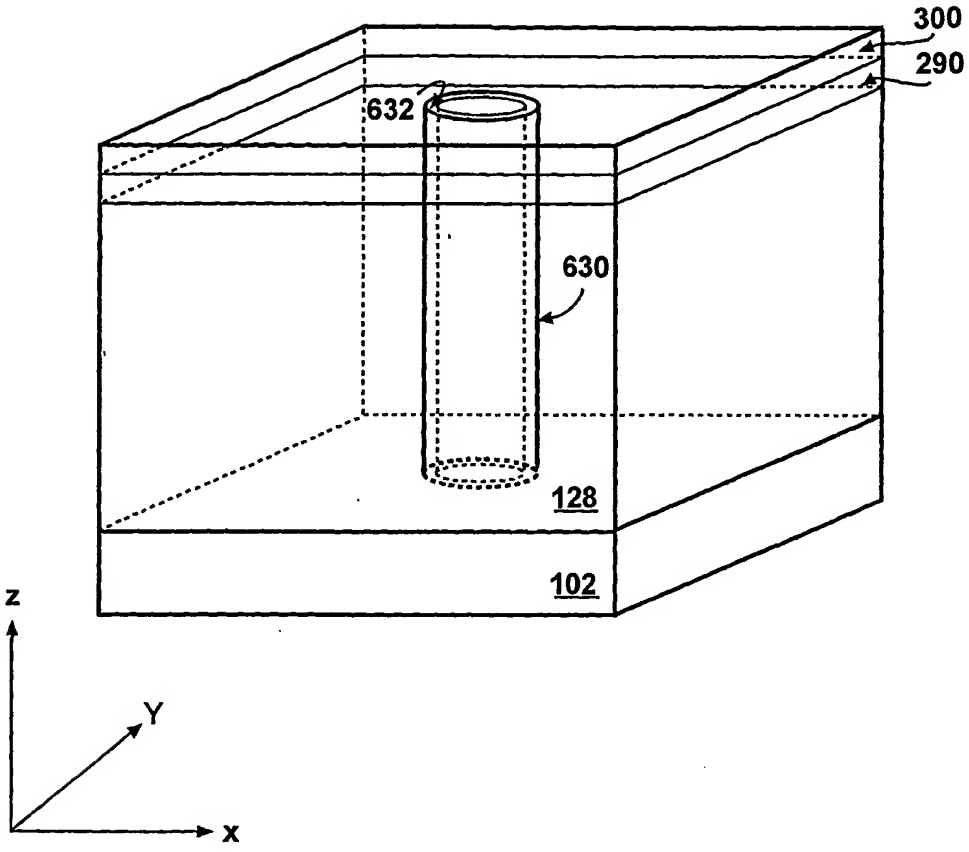


FIG - 13B

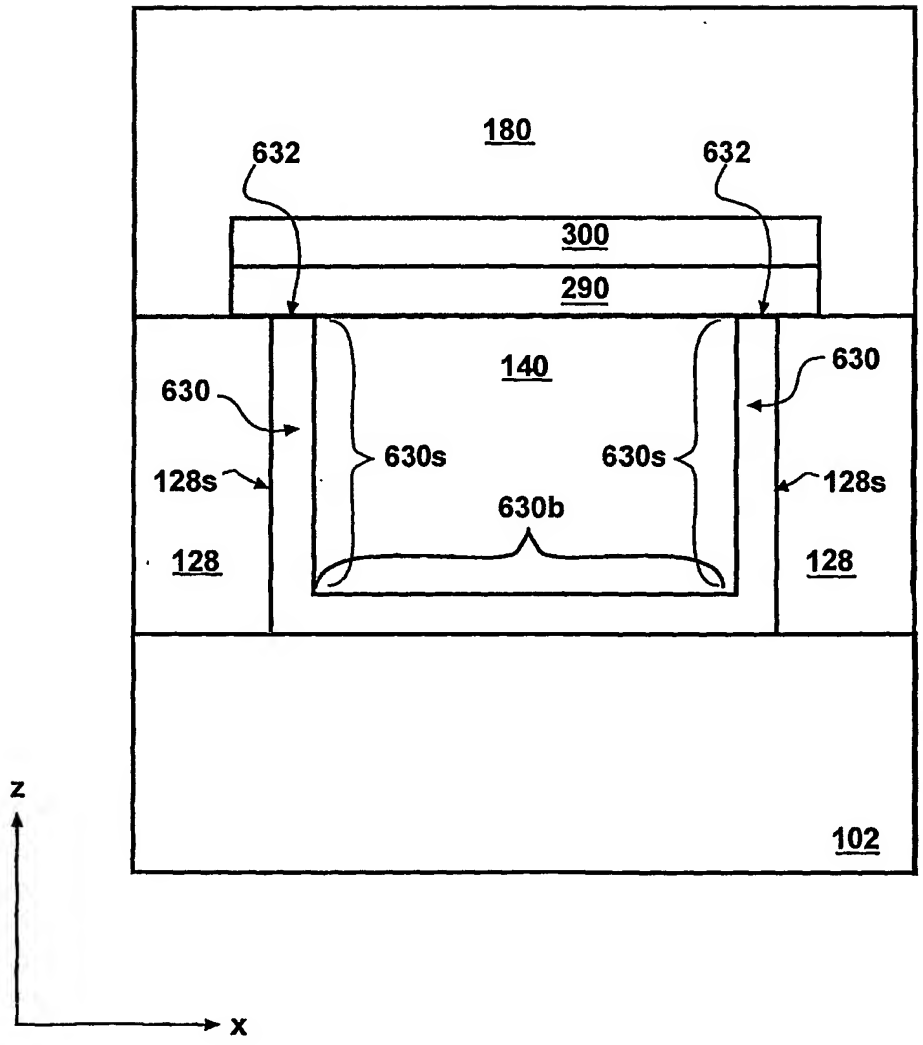

180
632
632
300
290
140
630
630
630s
630s
128s
128s
630b
128
128
102
z
x

FIG - 13C

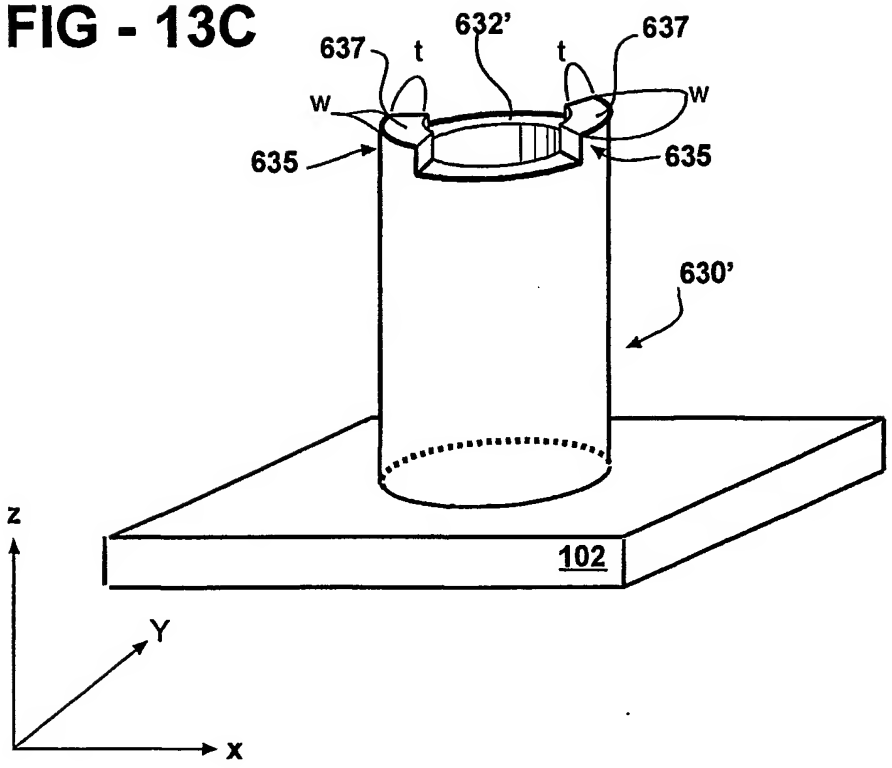


FIG - 13D

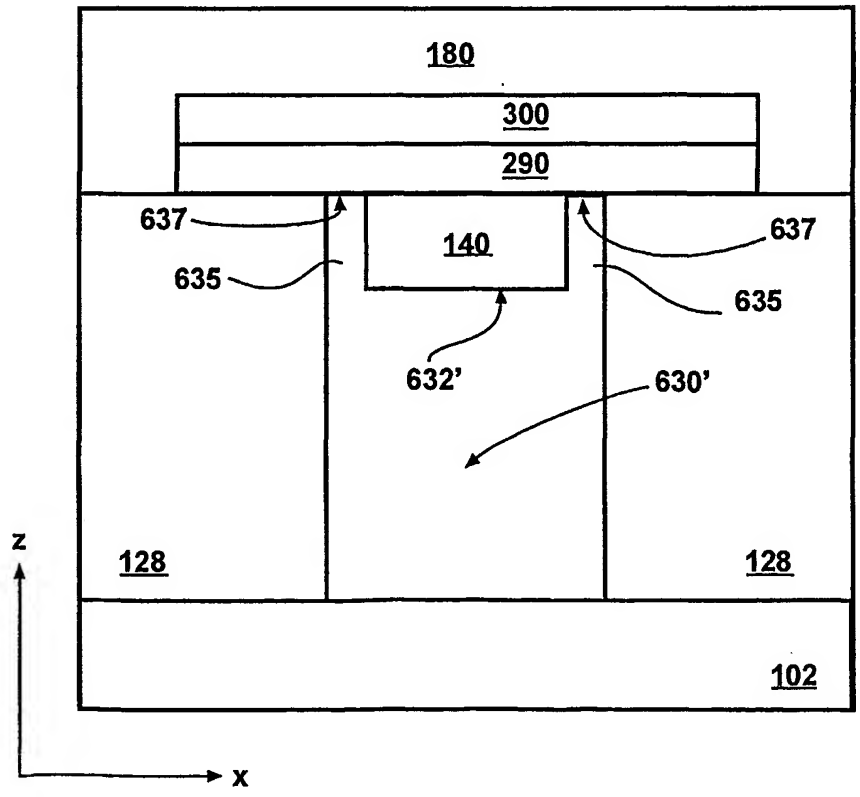


FIG - 14A

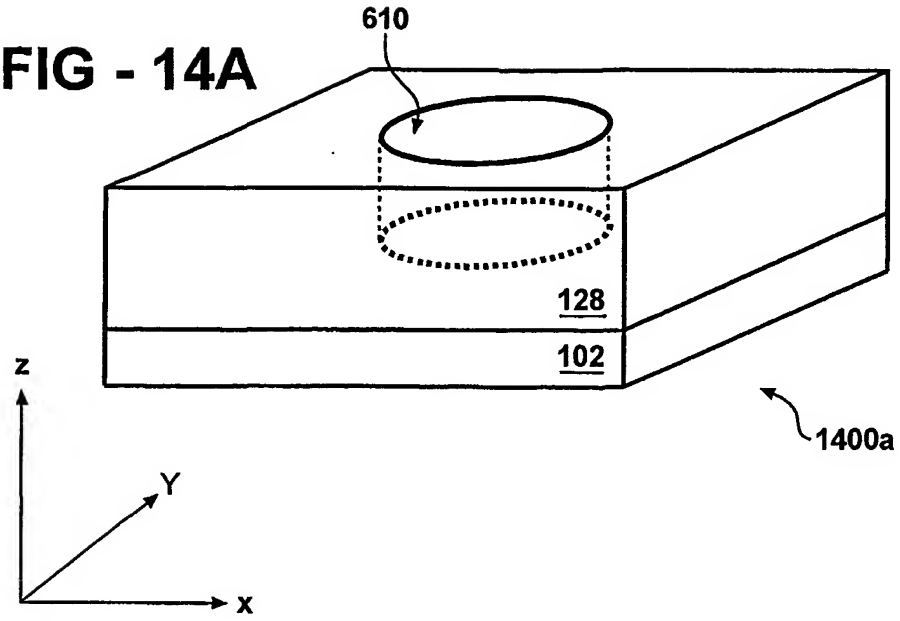


FIG - 14B

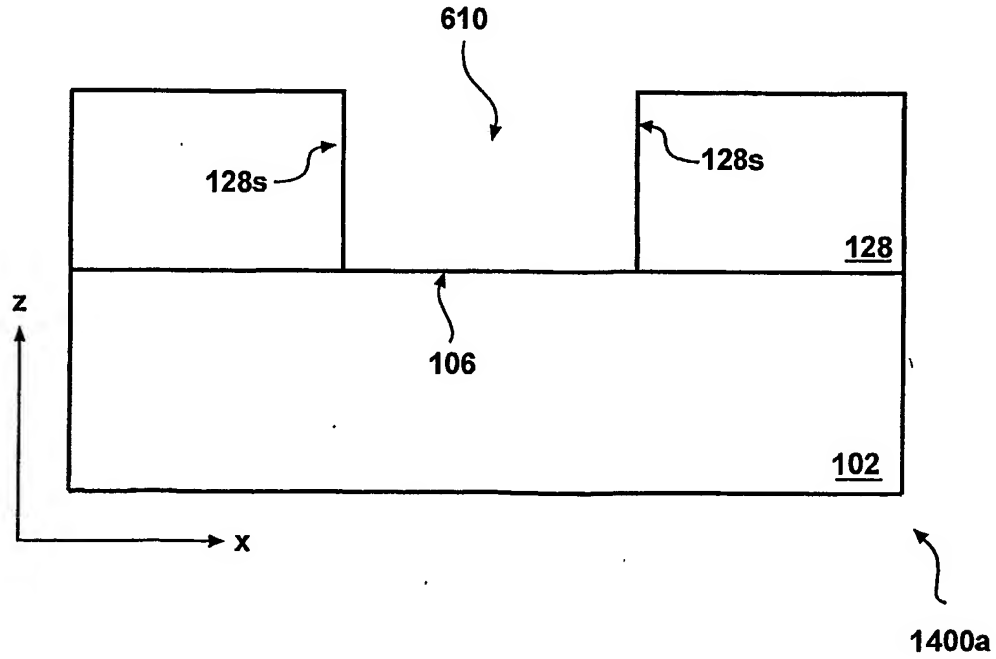
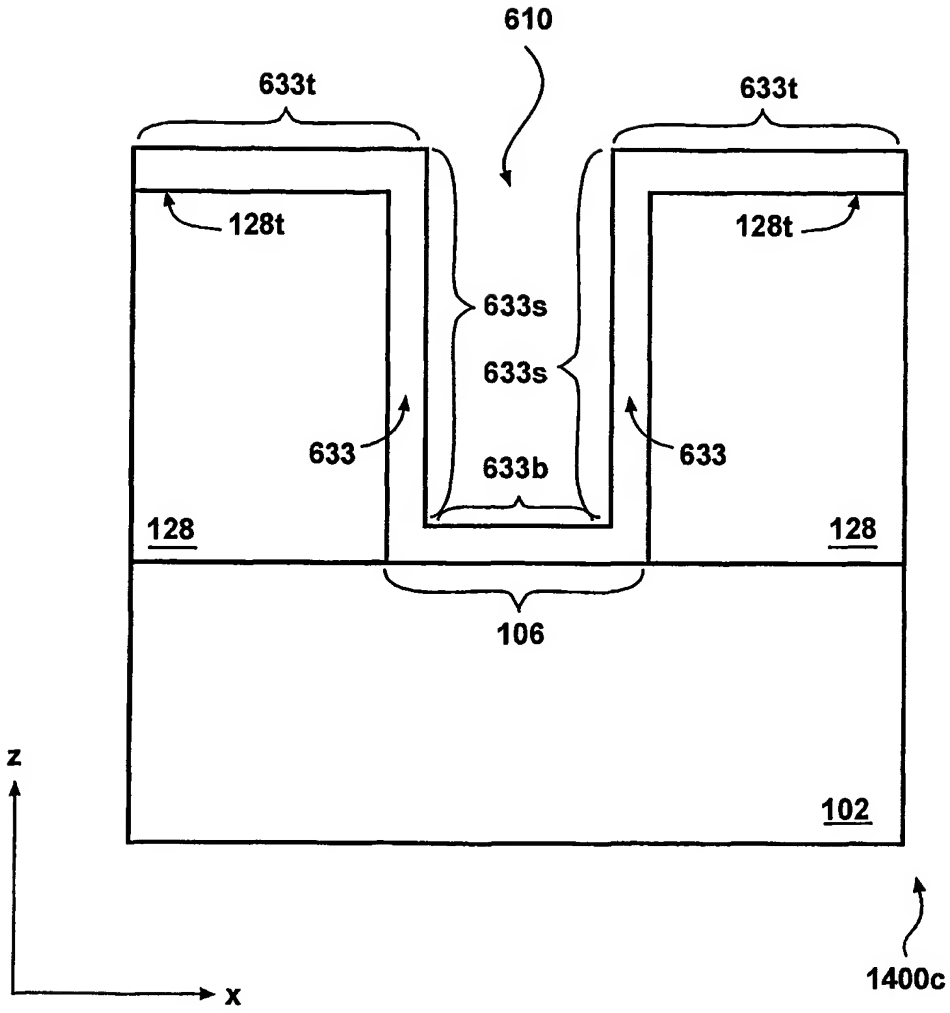


FIG - 14C


610
633t
633t
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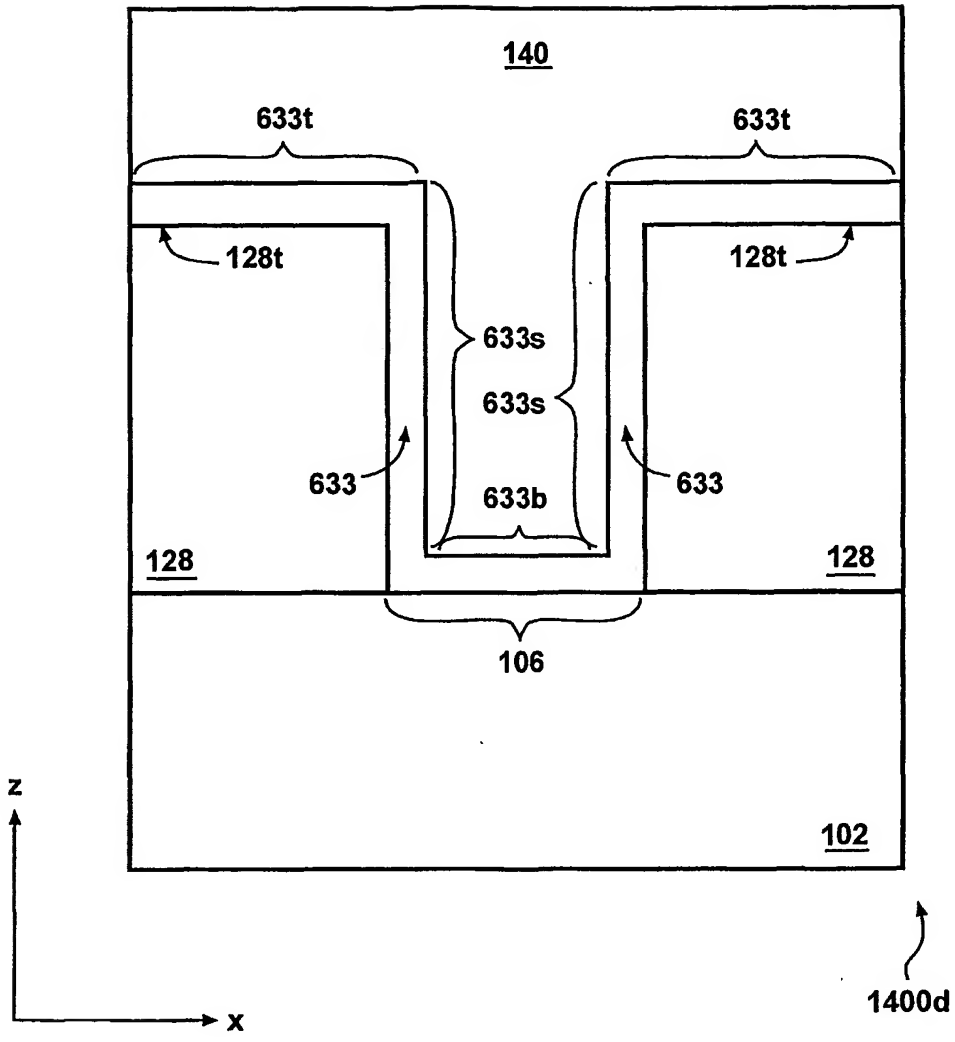
128t
633s
633s
633
633
633b
128
128
106
102
z
x
1400c

FIG - 14D


140
633t
633t
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128t
633s
633s
633
633
633b
128
128
106
102
z
x
1400d

FIG - 14E

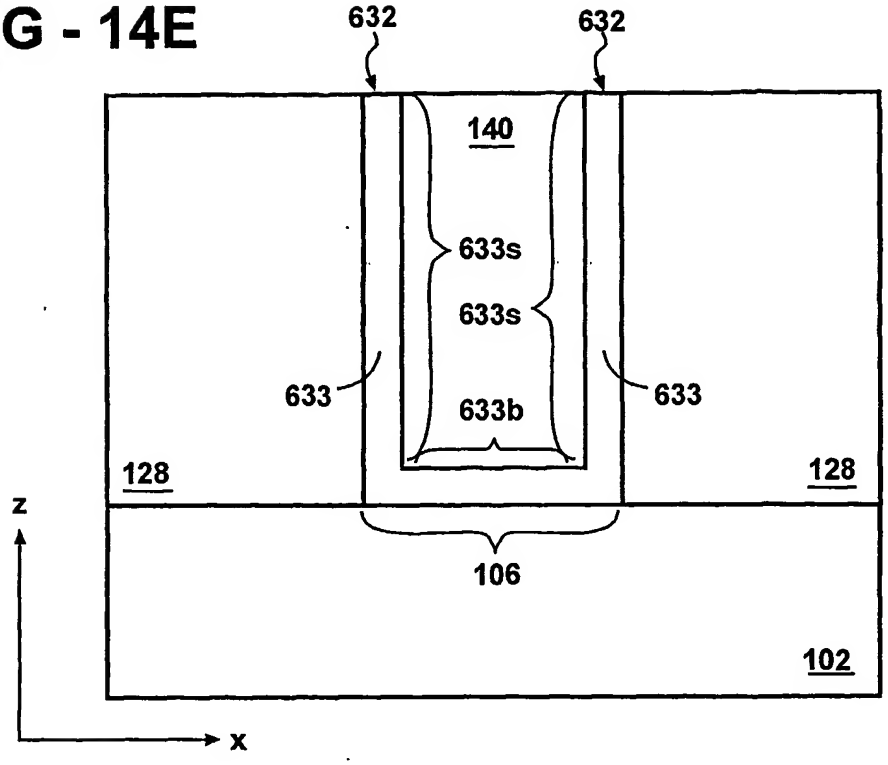


FIG - 14E'

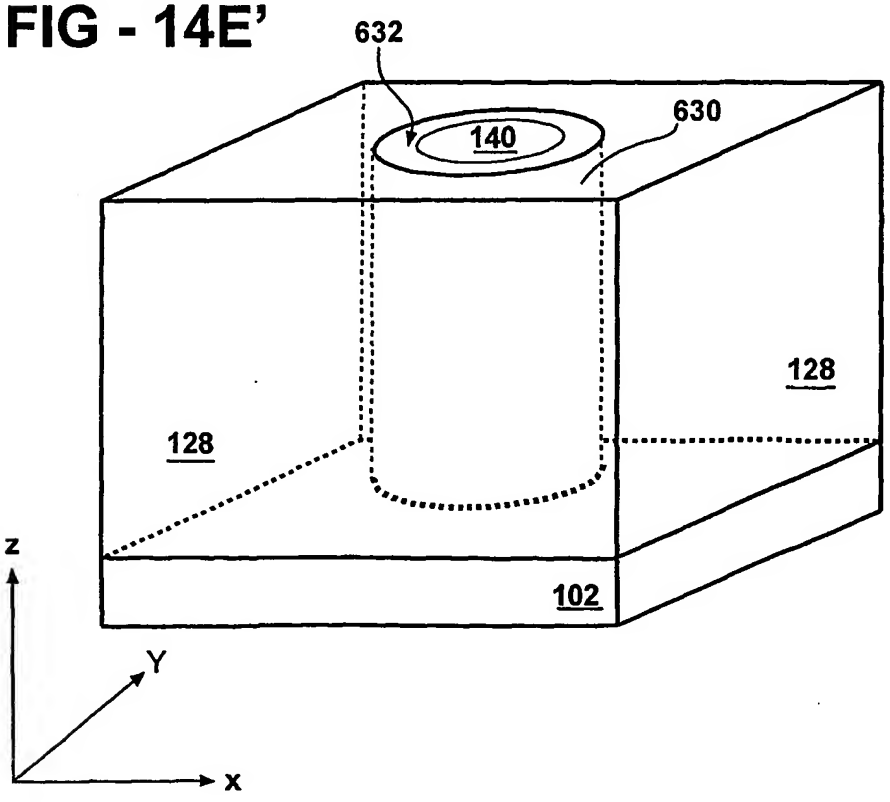


FIG - 14F

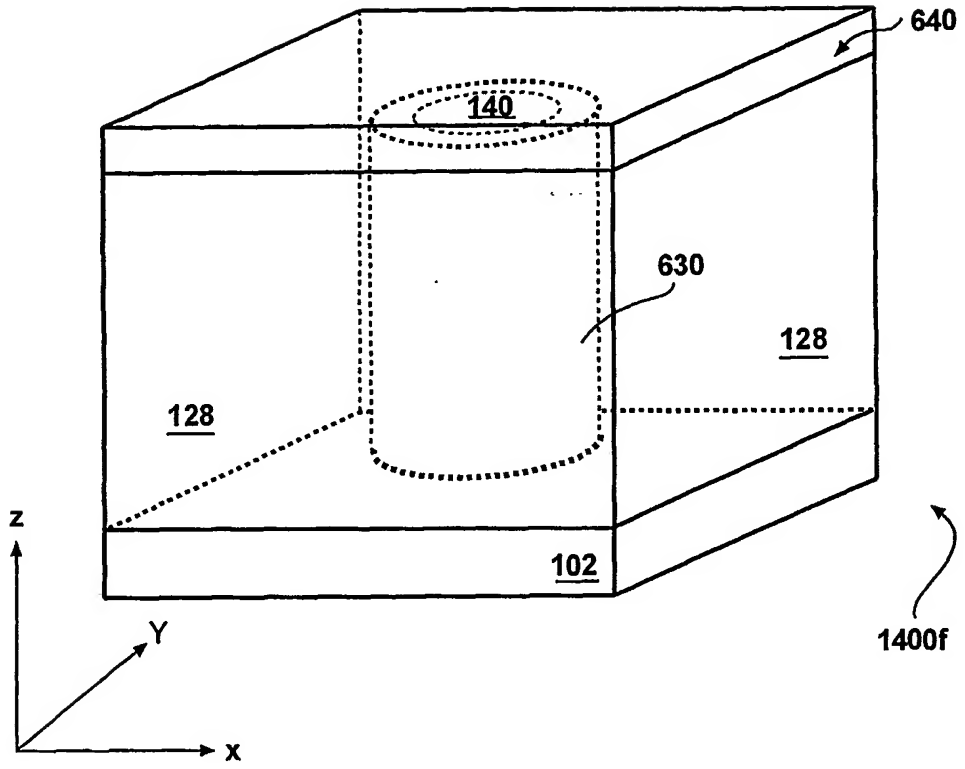


FIG - 14F'

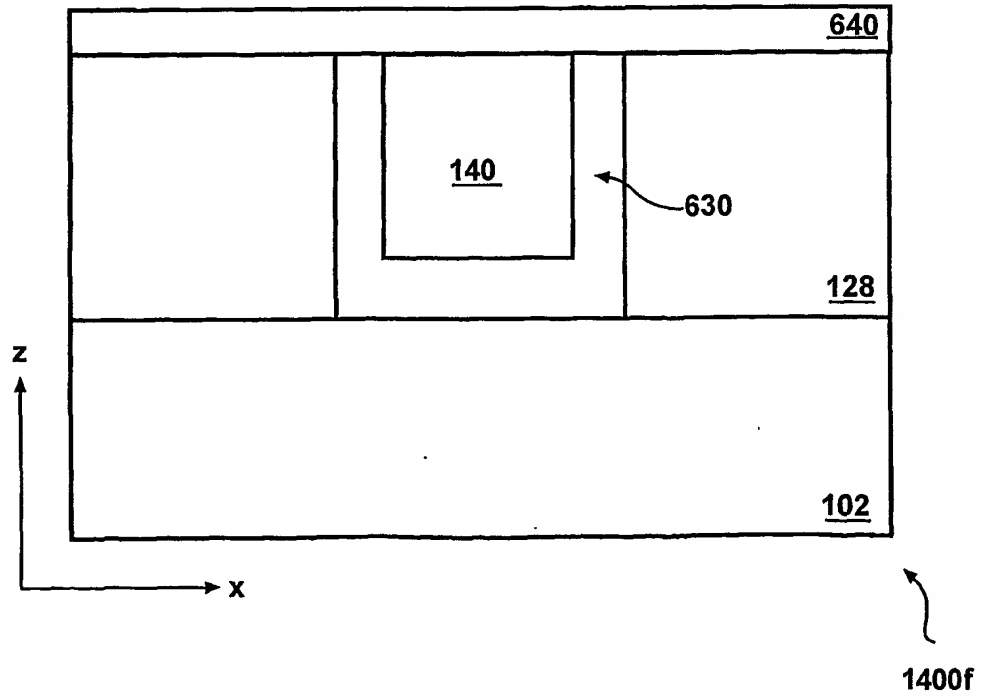


FIG - 14G'

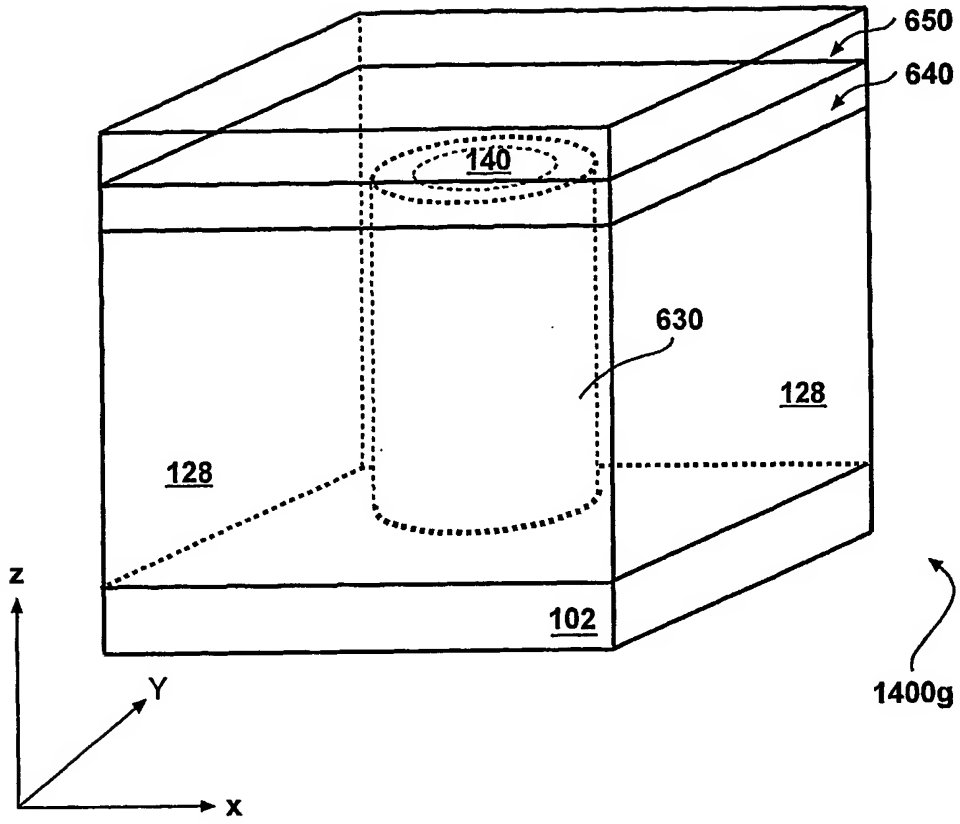


FIG - 14G

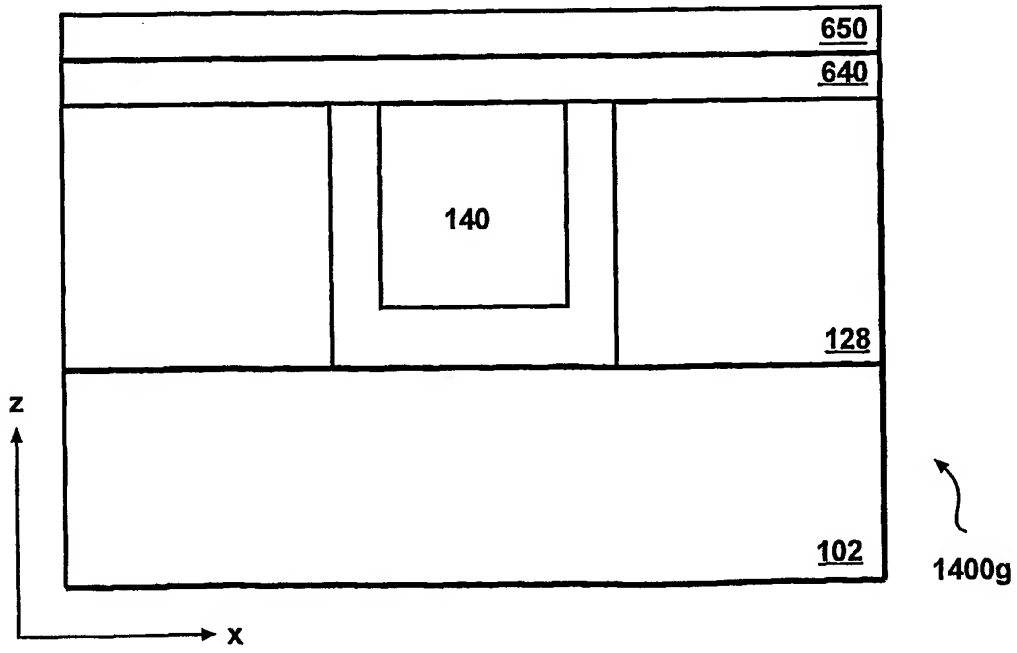


FIG - 14H

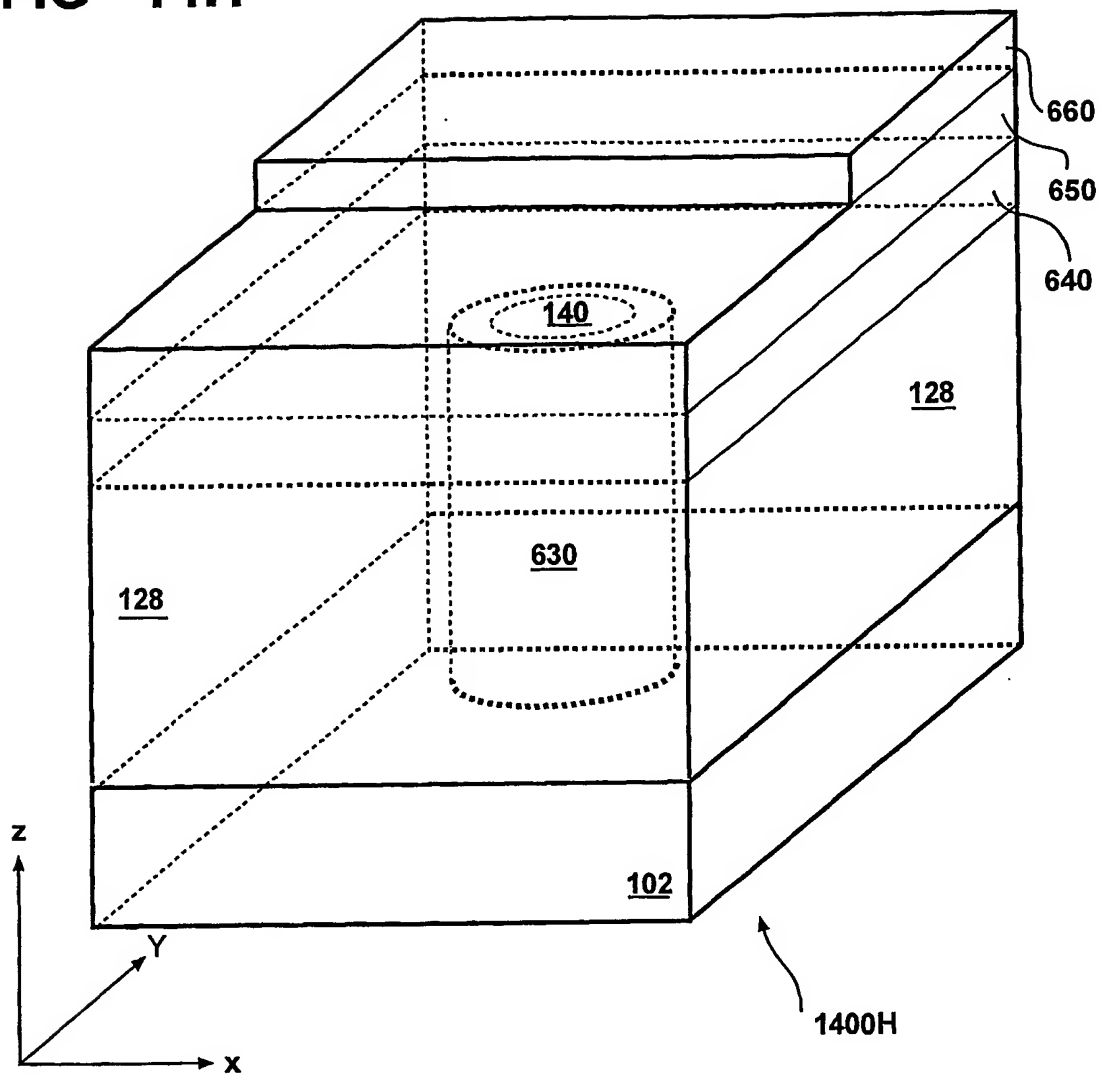
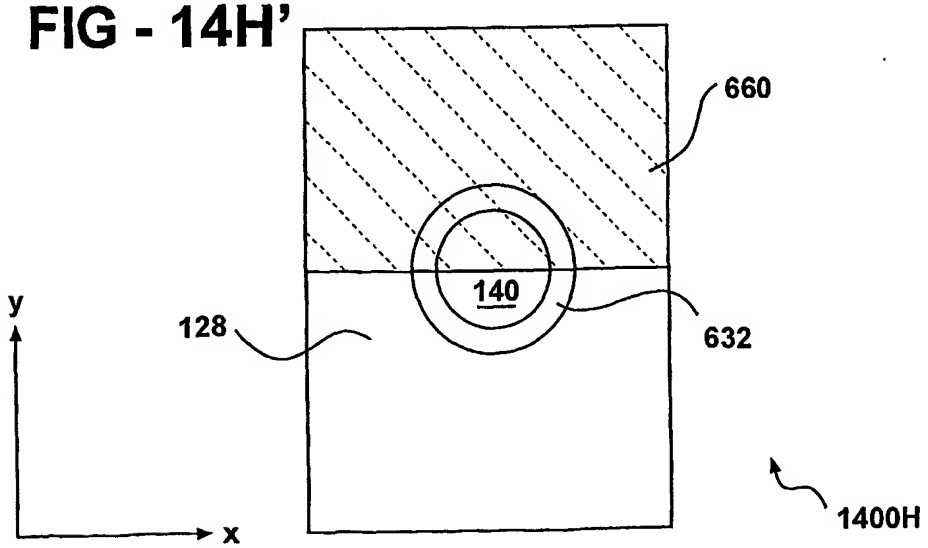


FIG - 14H'



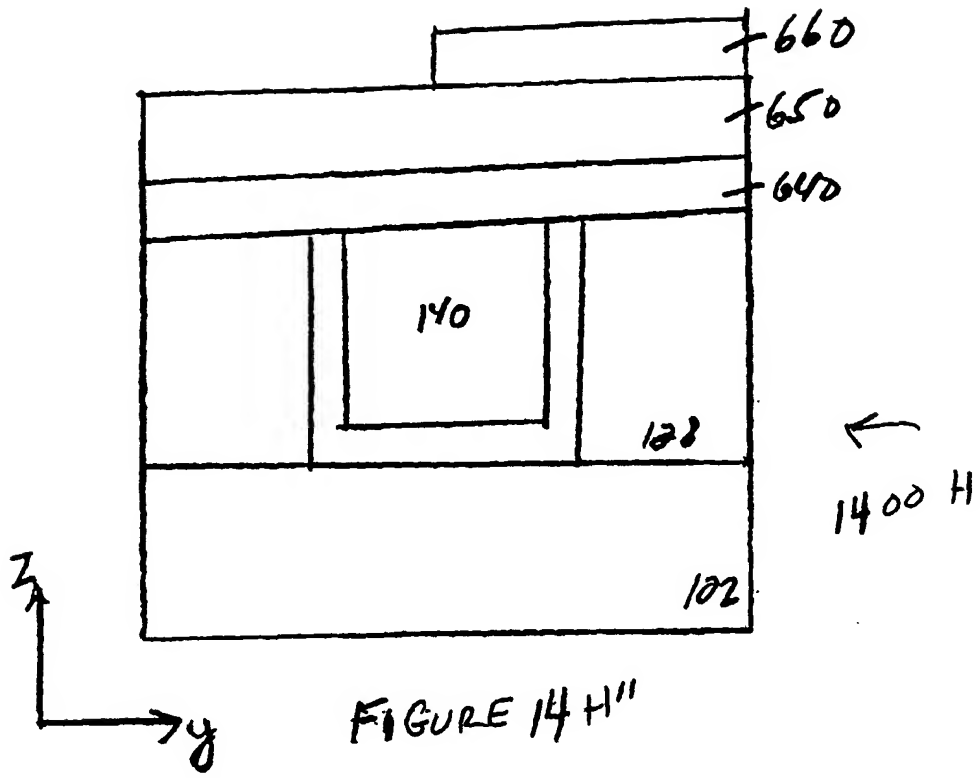


FIGURE 14H''

FIG - 14I

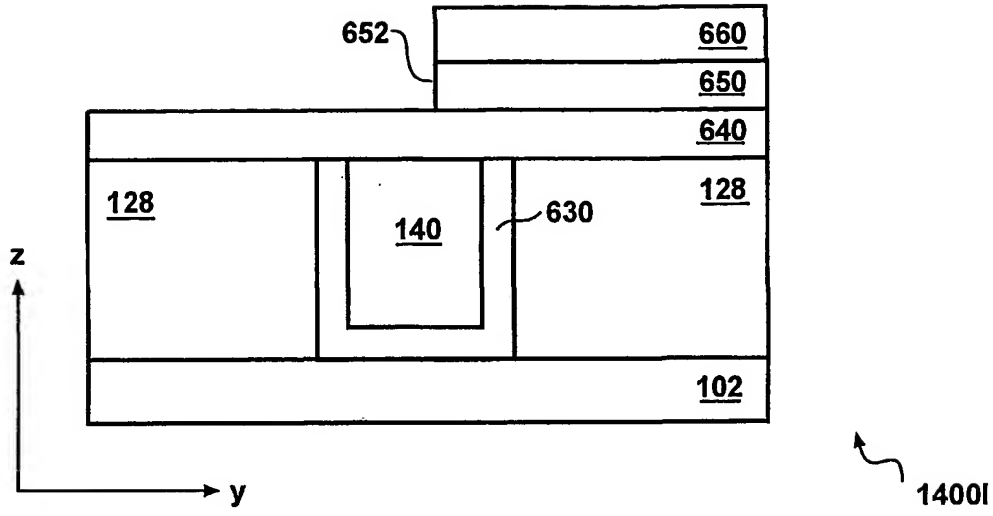


FIG - 14J

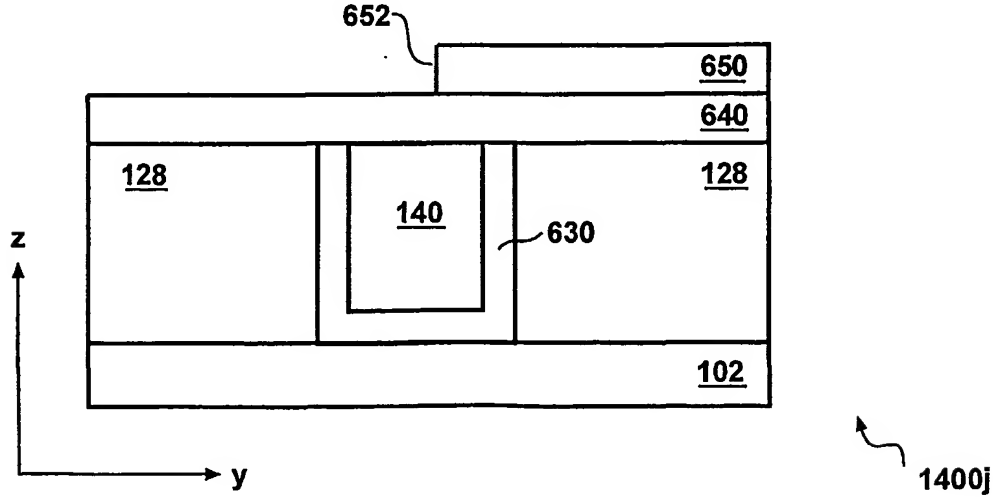


FIG - 14K

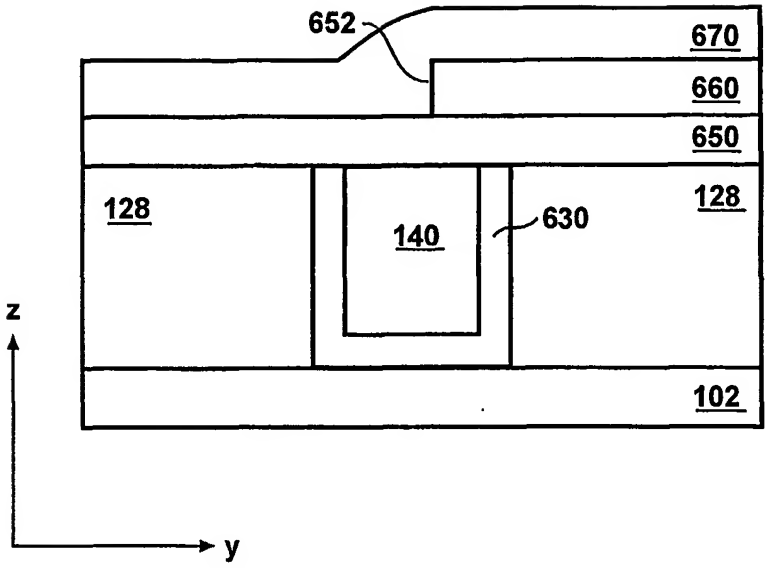
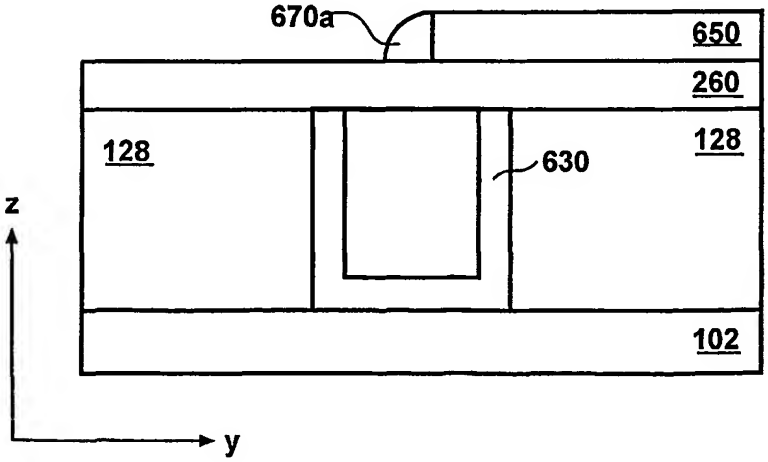


FIG - 14L



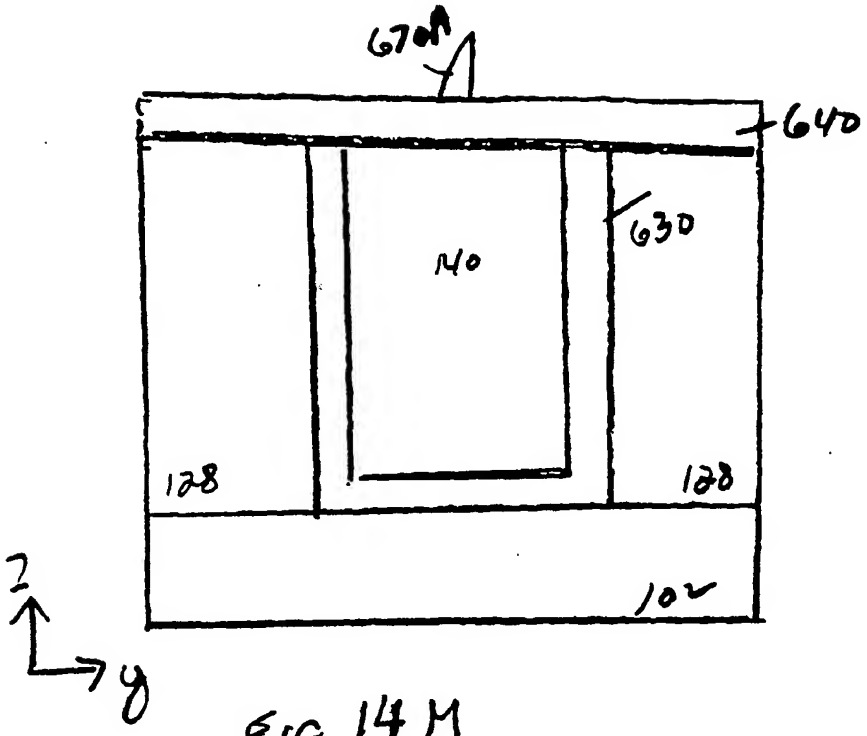


FIG 14M

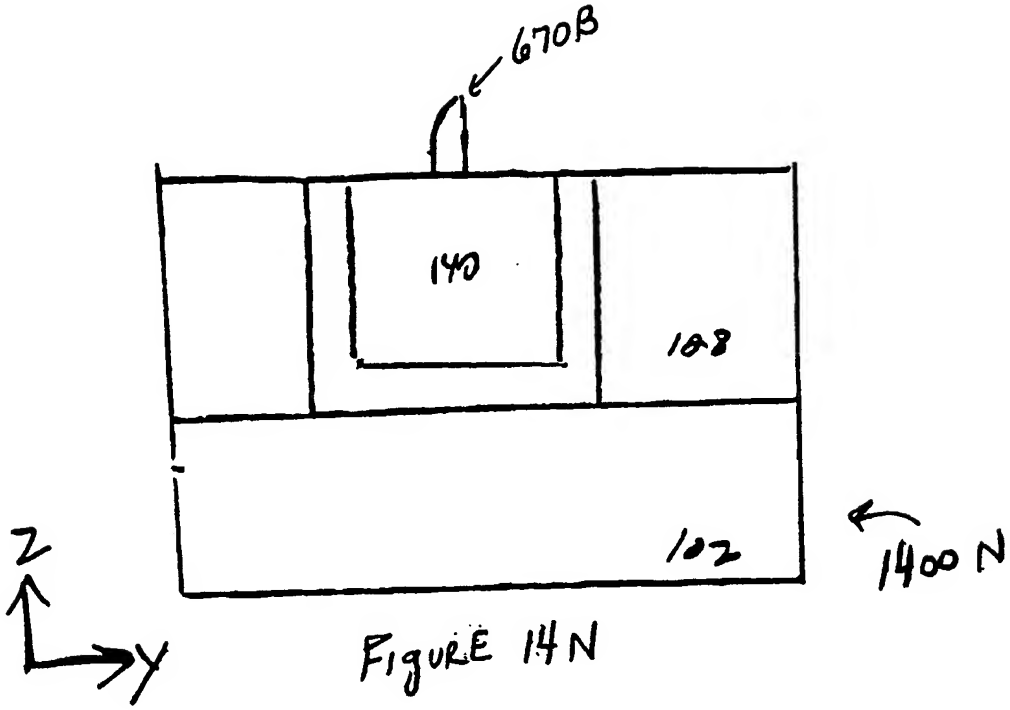


Figure 14N

FIG - 14N'

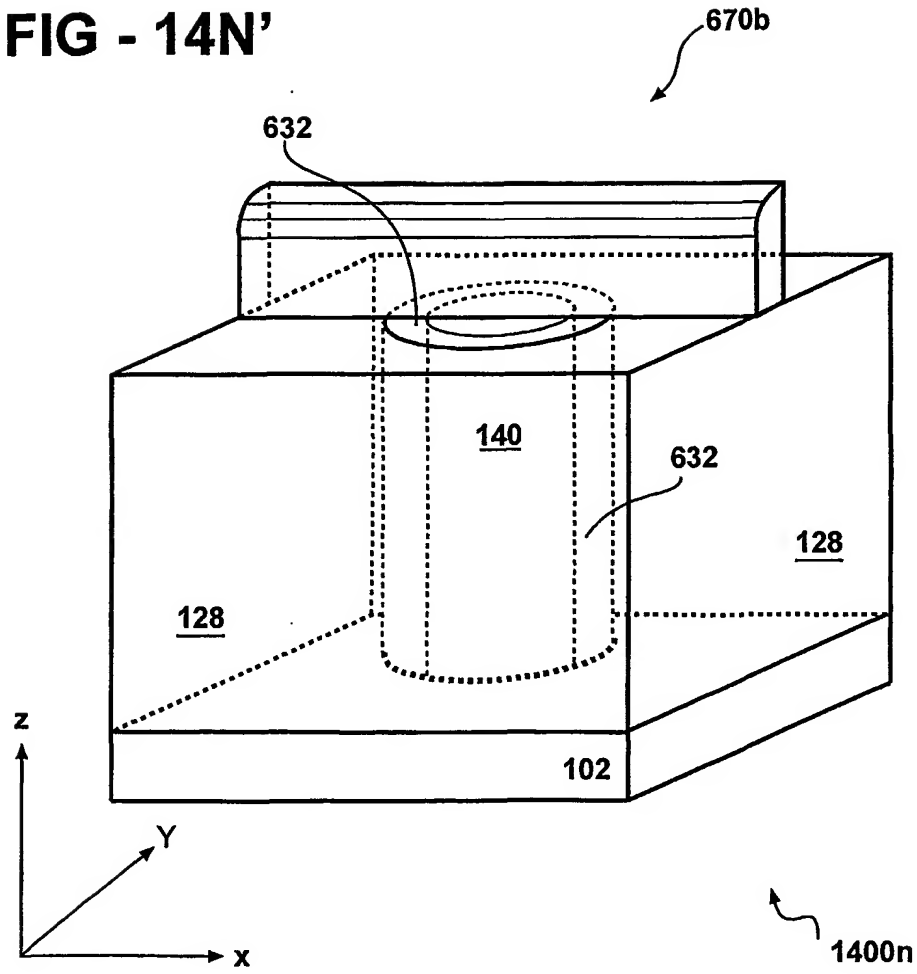


FIG - 14N"

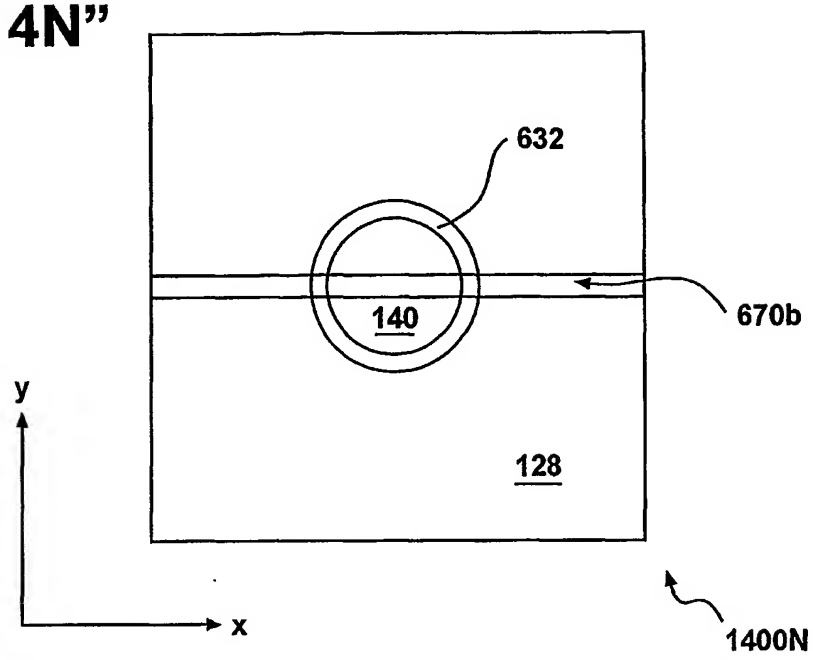


FIG - 14O

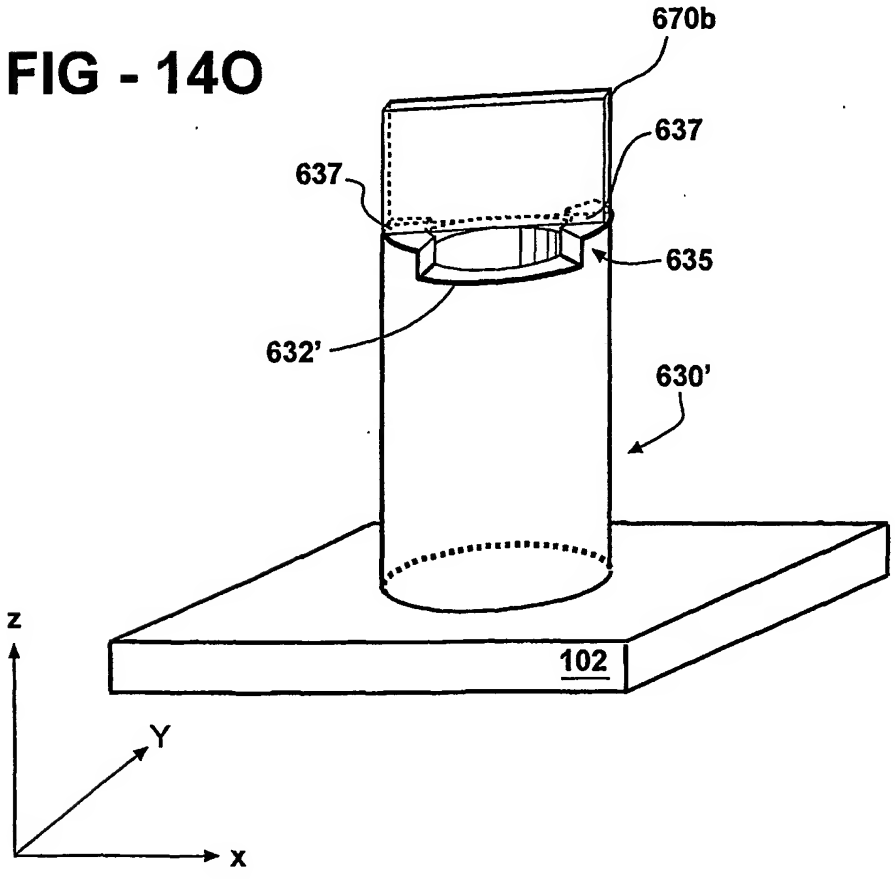


FIG - 14P

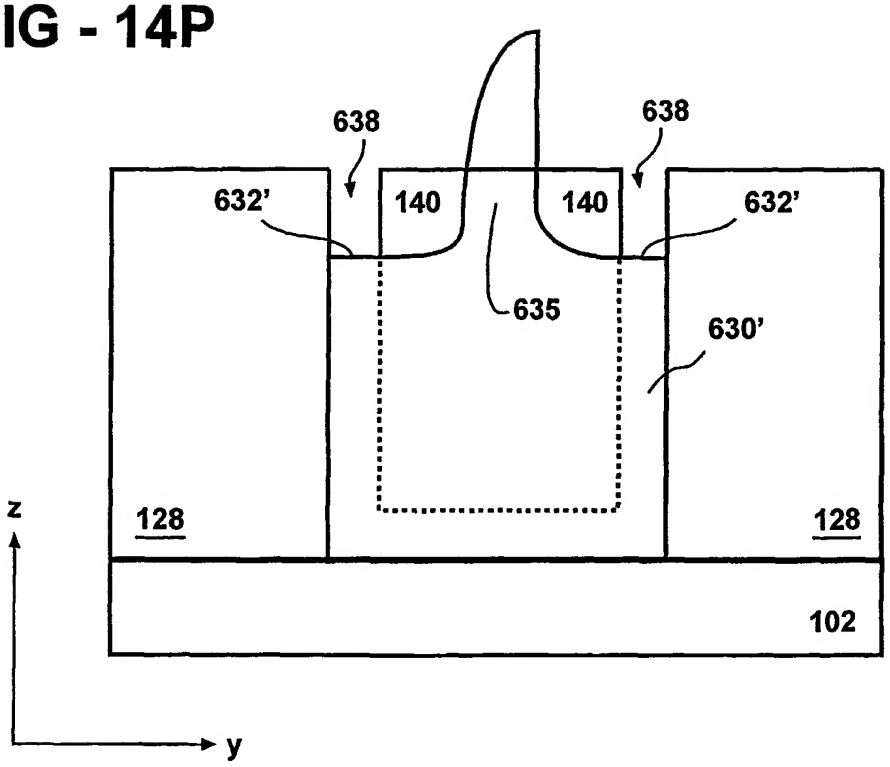


FIG - 14Q

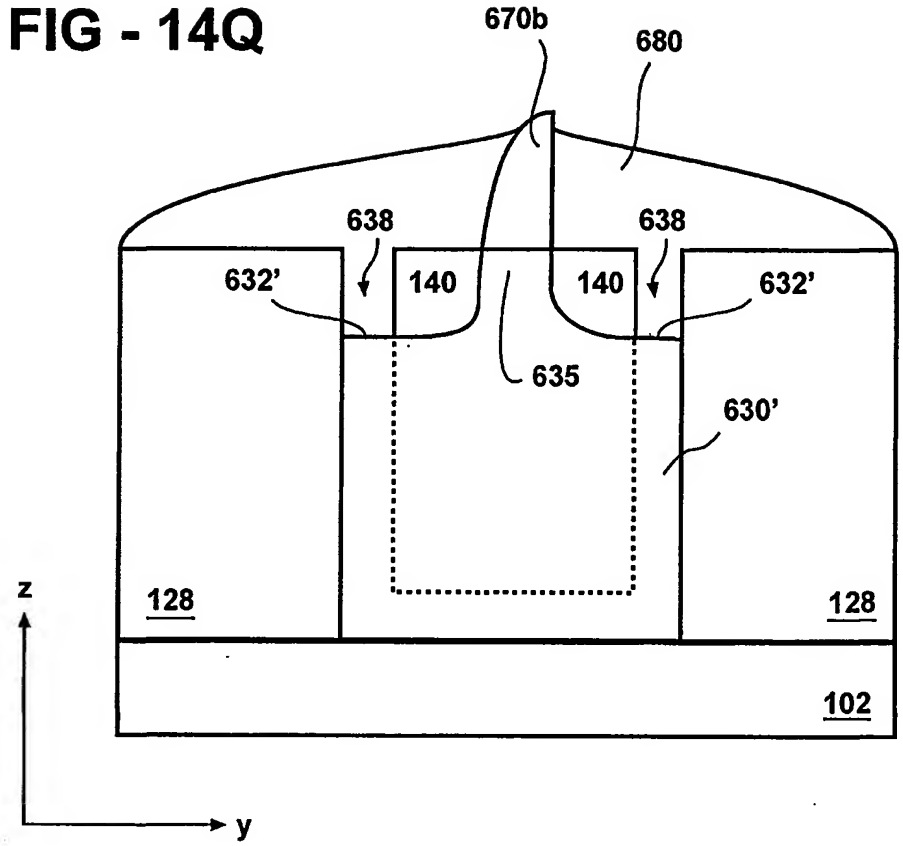


FIG - 14R

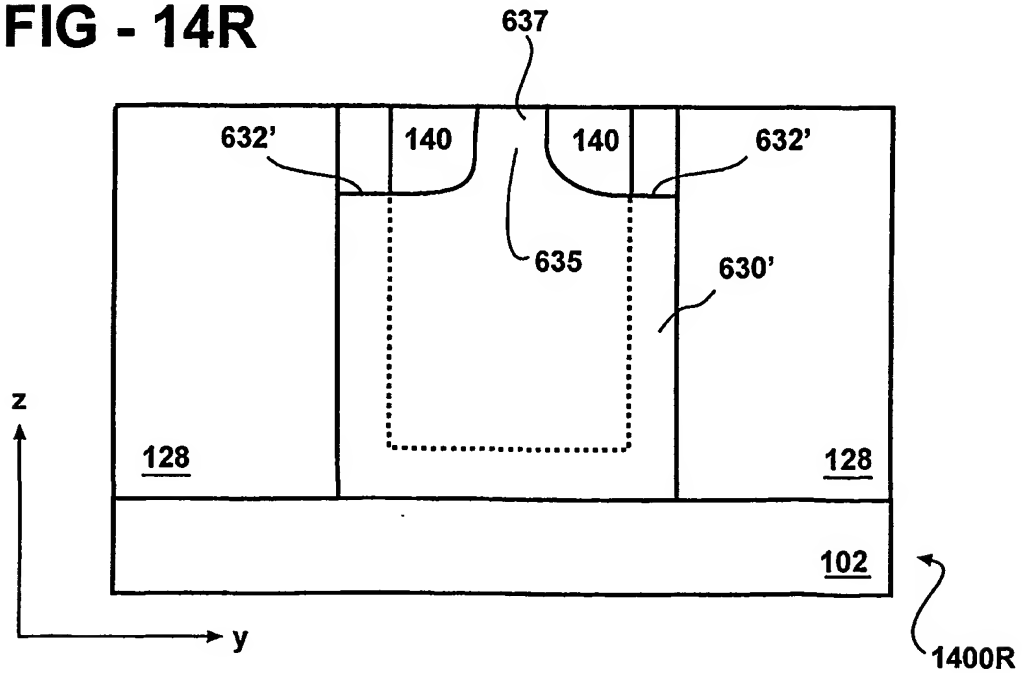


FIG - 14S

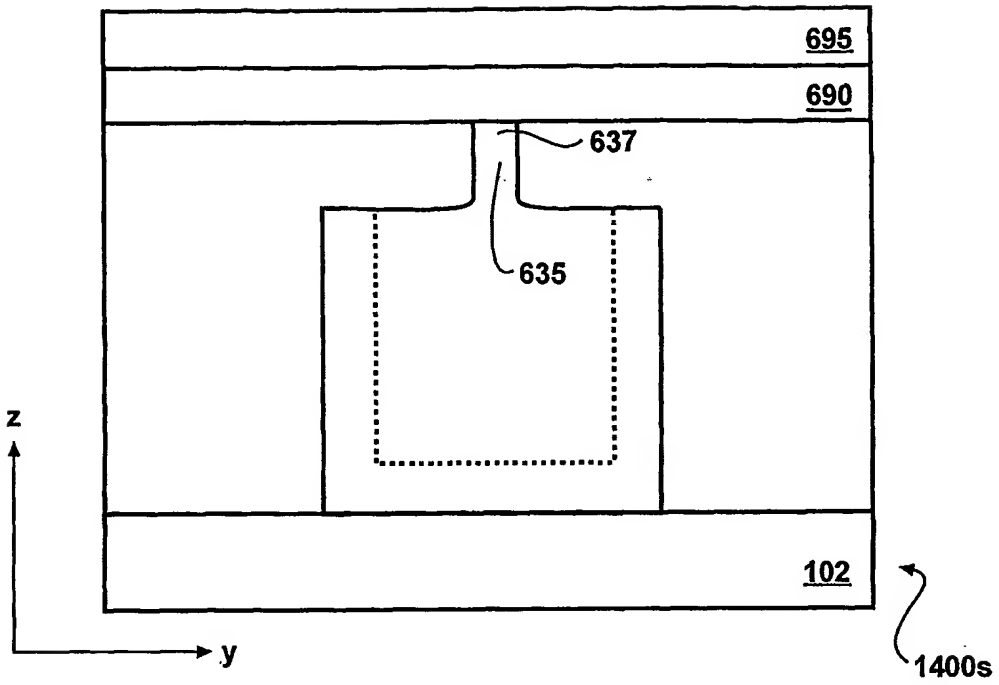


FIG - 14S'

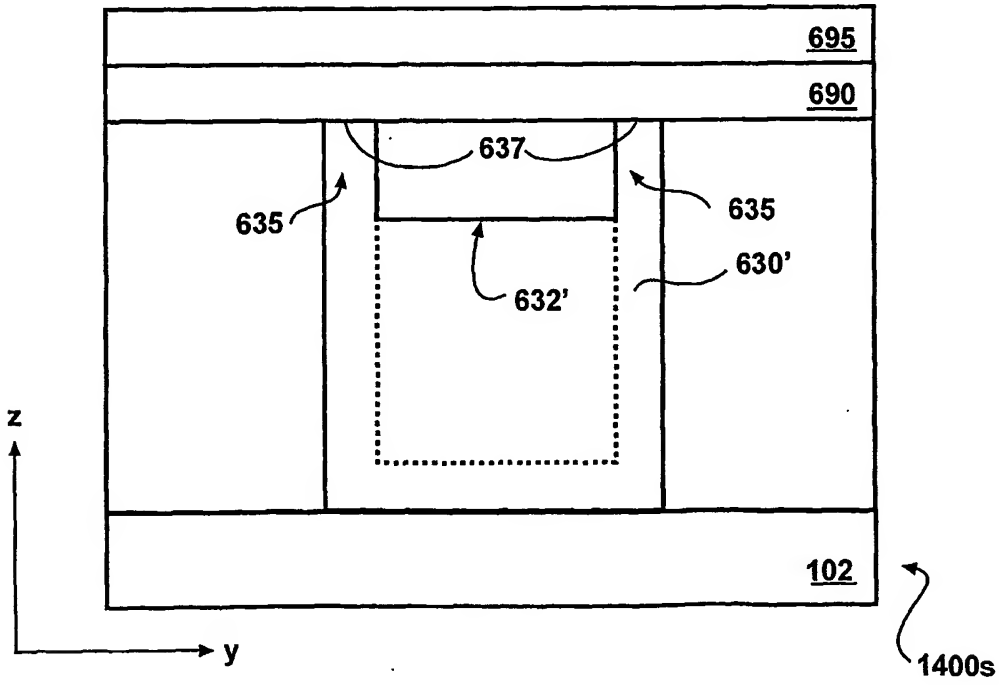
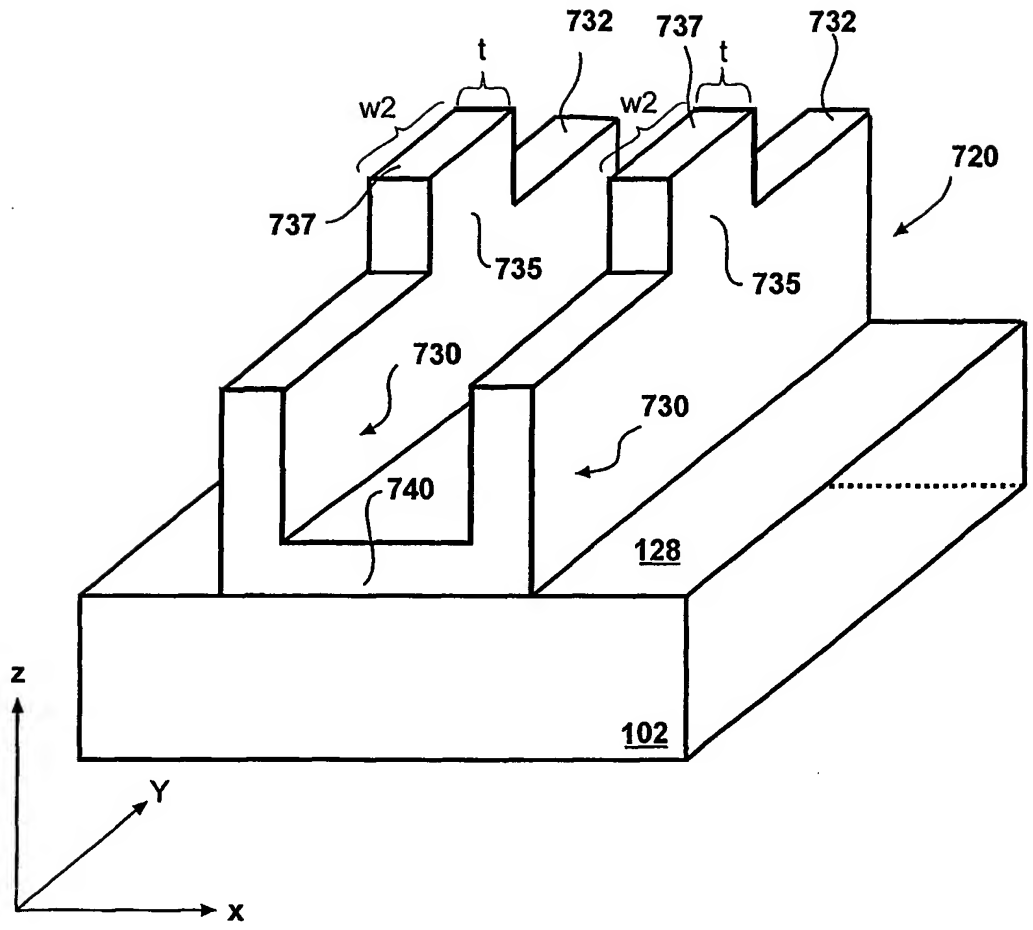


FIG - 15



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/22550

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 47/00
US CL :257/2, 3, 4, 5

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/2, 3, 4, 5

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO APS, EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X — Y — A	US 5,854,102 A (GONZALEZ et al) 29 December 1998 (29.12.1998), fig. 8; col. 7, lines 9-12; and col. 8, lines 8-13, 34-40.	1-6, 8-13 ——— 14-19, 29, 35, 36, 42 ——— second 6, 37-41
X — A	US 5,687,112 A (OVSHINSKY) 11 November 1997 (11.11.1997), fig. 2; col. 9, lines 6-14; col. 14, lines 25-40, 45-50; and col. 15, lines 1-2, 35-45.	1-6, 8-9, 13-17, 20, 26, 28-31, 35, 43-45 ——— 21-25, 27, 32-34, 46-48

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 13 SEPTEMBER 2001	Date of mailing of the international search report 01 NOV 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer PHAT XUAN CAO Telephone No. (703) 308-4917

Form PCT/ISA/210 (second sheet) (July 1998)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/22550

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,414,271 A (OVSHINSKY et al) 09 May 1995 (09.05.1995), fig. 1; col. 11, lines 28-35; col. 16, lines 31-35, 46-51.	1-9, 13-19, 29, 35 ------- 36, 42
X	US 5,714,768 A (OVSHINSKY et al) 03 February 1998 (03.02.1998), fig. 1; col. 3, lines 44-56; col. 6, lines 48-60; and col. 8, lines 51-64.	1-9, 13-17, 29, 35
X --- Y --- A	US 6,064,084 A (TANAHASHI) 16 May 2000 (16.05.2000), figs. 2A, 2B, 2C.	43, 49 ------- 14-19, 29, 35-36, 42 -------- 50-54